INTRODUCTION

RP2350 is a high-performance, secure, low-cost, and easy-to-use microcontroller launched by Raspberry Pi. It has a large capacity on-chip memory, a symmetrical dual core processor, a deterministic bus structure, and a rich set of peripherals, and is equipped with our unique programmable I/O (PIO) subsystem, providing unparalleled power and flexibility for professional users. RP2350 has detailed documentation, a comprehensive MicroPython port, and a UF2 bootloader in ROM, providing the lowest entry barrier for beginners and amateur users.

RP2350 is a stateless device that supports cache in place execution of external QSPI memory. This design decision allows you to choose the appropriate density of non-volatile storage for your application and benefit from the low price of commodity flash components.

RP2350 is manufactured using modern 40nm process nodes and features high performance, low dynamic power consumption, and low leakage. It also provides multiple low-power modes and supports long-term operation powered by batteries.

MAIN FUNCTIONS

Dual Cortex-M33 or Hazard3 processors with frequencies up to 150MHz

520KB multi group high-performance SRAM

Supports up to 16MB of off chip flash memory through a dedicated QSPI bus

dma controller

Fully connected AHB crossbar switch

On chip programmable LDO generates core voltage

2 x on-chip PLLs for generating USB and kernel clocks

30 GPIO pins, of which 4 can be used as analog inputs

2 x UART

2 x SPI controllers

2 x I2C controllers

24 x PWM channels

USB 1.1 controller and PHY, supporting both hosts and devices

3 x Programmable IO (PIO) blocks, totaling 12 state machines

SAFETY

RP2350 has a comprehensive security architecture built around Arm TrustZone for Cortex-M, including the following features:

Support signature startup

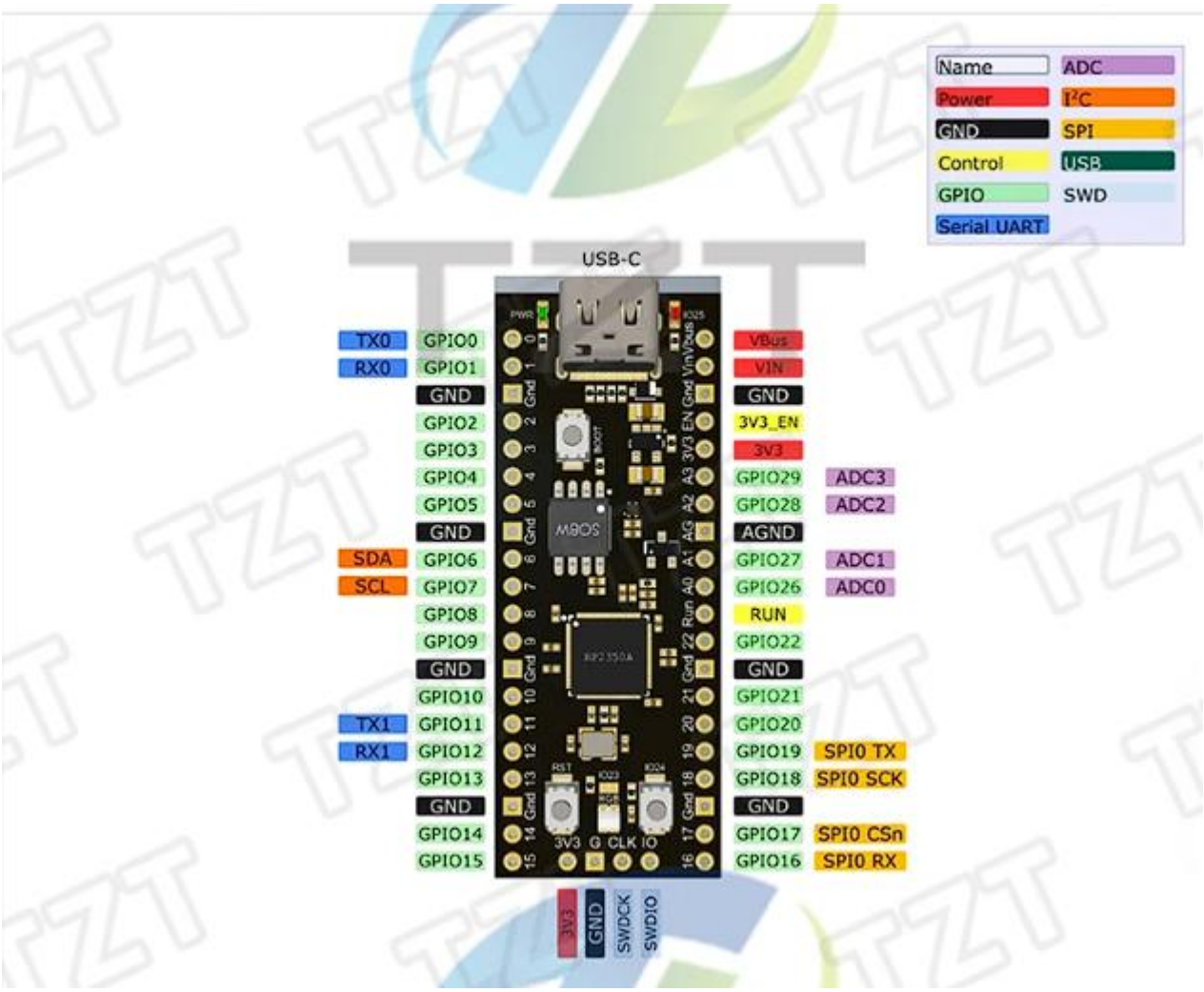
8KB on-chip anti fuse one-time programmable (OTP) memory

SHA-256 Acceleration

Hardware True Random Number Generator (TRNG)

ARCHITECTURE SWITCHING

RP2350 includes a pair of open hardware Hazard3 RISC-V cores that can replace Cortex-M33 cores at startup. Our boot ROM can even automatically detect the architecture of the second stage binary file that has been built and restart the chip to the corresponding mode. All functions of the chip can be used in RISC-V mode, except for a few security features and a double precision floating-point accelerator.



Power
"RAW" Pin: 12V Max at ~300mA
USB: 5V at ~500mA (default), dependent on USB Port
"3V3" Pin: Regulated 3.3V
I/O Logic Levels: 3.3V

USB
USB 1.1 Device/Host

RP2350A
Absolute maxiumum VCC: 3.3V
Dual ARM Cortex M33 or Hazard3 (up to 150MHz)
ROM: 16kB (fixed at time of silicon is manufactured)
Internal SRAM: 520kB
ADC: 12-bit
PWM: 16-bit

25Q128
External Flash Program Memory: 16MB

Notes
- The pins on the RP2350A can be muxed! For more information on the multiplexed pins, check out "section 1.2.3 GPIO Functions" of the RP2350 datasheet.