QS0503F2-Process Change Notice Form Rev. E

01052201

PCN Number: 01052201	**PCN Date:** 23May01	**Effective Date:** 05Oct01
Title: Si3210 ProSLIC Revision E Introduction and Revision 1.0 ProSLIC Datasheet		
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PCN Type:	☐ *Fabrication*	☐ *Package*	☐ *Discontinuance*
■ *Major*	☐ *Assembly*	■ *Product Revision*	*Last Order Date:*_____
☐ *Minor*	☐ *Test*	☐ *Other*	

PCN Details

Description of Change: Silicon Laboratories is pleased to announce revision E of the Si3210 ProSLIC and revision 1.0 of the ProSLIC data sheet. Performance and feature improvements to revision E are detailed in the attached document. Fab and assembly processes are unchanged.

Reason for Change:

1. Increased system software robustness. Revision E of the ProSLIC has removed user access to some dc-dc converter control bits in direct registers 66, 92, 93 to increase system integrity to inappropriate register settings in the event of unstable system software.
2. Data sheet updates, which are listed in section ”Document Changes from Revision 0.9 to 1.0” on pg. 124 of the revision 1.0 datasheet
3. Eliminate revision B errata items.
4. Improved ESD performance. Revision D passes 2000 V human body model. Revision B passes 1250 V human body model, but fails at 1500 V.
5. Additional feature and performance enhancements in attached document.

Product Identification:

The product revision can be identified from the tracecode mark:

0 1 0 9 D C C A 1 3
| | | | | | |
| | | | | | Serial Number
| | | | | Optional/Test site
| | | | Assembly site
| | | Fab Site/Process
| | Die Revision: “B” = revision B silicon; “D” = revision D silicon; “E” = revision E silicon
Date Code (YY – Year; WW – work week)

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Projected Implementation Date:

This PCN will become effective 90 days after the PCN issue date, unless the customer approves for early release.

Customer approval for early release:

Early Release Date: _____ Signature: _____

Name: _____ Company: _____

Title: _____ Date: _____

Respond to Roger Wood at fax: 512-416-9669 or at email: raw@silabs.com with approval information.

Qualification Data:

See attached qualification report.

Si3210 ProSLIC™ Revision E Enhancements

Performance Differences

1. **DC/DC converter register enhancements** – Revision E of the ProSLIC contains enhancements to programmable registers to increase system integrity in the presence of unstable user system software. Revision E protects software registers associated with the dc-dc converter control and monitoring circuitry by preventing the user from writing inappropriate values to these registers (direct registers 66, 92, 93) which can potentially cause circuit damage to the system.

    - The EXTBAT register bit (direct register 66, bit 2) has been removed from the Si3210 memory map.
    - The DCPOL register bit (direct register 93, bit 5) has been changed to be read-only. The Si3210 and Si3210M offer identical operation with the exception of the DCFF pin. DCFF output is opposite in polarity to the DCDRV pin for the Si3210 and the same polarity for the Si3210M.
    - Bit 6 of the DCN register (direct register 92) has been fixed to logic one, which partitions the available PWM frequencies into two regions: 64kHz to 85kHz used for BJT switching; and 129kHz to 256kHz for MOSFET switching.

2. **PLL control** – Revision E disables the ability to power down the PLL circuitry. The PLLOF bit (register 14, bit 0) cannot be written.

3. **Revision control register** – The revision number identification bits, RNI[3:0] in register read "0010" for Rev. B, "0100" for Rev. D, and "0101" for Rev. E.

4. **Feature enhancements** – Revision E (and revision D) contains feature enhancements that are described in the latest datasheet (revision 1.0) and listed below. They can be enabled individually in direct register 108.
    a. Current limit increase during ringing
    b. FSK generation enhancement mode
    c. DC-to-DC converter control speedup
    d. Impedance internal reference resistor disable
    e. Battery switch debounce
    f. Voltage-based loop closure detection
    g. DC-to-DC converter squelch
    h. Loop closure hysteresis
5. **Overload compression** – Revision E (and rev. D) has improved overload compression performance. Rev. E (and rev. D) has the same compression performance as Rev. B, but can do so with 1.5V less of tip-to-ground overhead voltage, V_{CM}.
6. **Calibration battery voltage** – For Rev. B, DC-DC converter calibrations are run at VBAT = -75V. For Rev. E (and rev. D), DC-DC converter calibrations are run at the voltage defined by VBATH (direct register 74) at the time of calibration execution.
7. **Longitudinal balance performance** – Revision E (and rev. D) has improved intrinsic longitudinal balance that can be realized at a system level when high beta or matched beta PNP linefeed transistors (Q1 and Q2) are used. This increased performance is quantified in the AC Characteristics section of the datasheet.
8. **Improved pulse metering distortion** – Revision E (and rev. D) has improved pulse metering signal generation with less than 10% distortion.
9. **Calibration settling times** – Revision B and E/D have different default calibration settling times: Revision B = 60ms, Revision E/D = 300ms.
10. **Calibration routines** – All calibration routines are functional in revision E (and rev. D). For revision B, calibrations should be followed according to the revision B errata document.
11. **Automatic ring trip state transition** – For revision E (and rev. D), the mode to automatically transition to the off-hook state upon a ring trip detect is functional as described in the datasheet. For revision B, ring trip detection should be performed according to the revision B errata document.
12. **PCLK and FSYNC jitter tolerance** – Revision E (and rev. D) silicon has improved PCLK and FSYNC period jitter tolerance to +/- 120ns. Jitter tolerance for revision B is about +/- 10ns.

13. **DC-to-DC converter overhead voltage** – Revision E (and rev. D) has a programmable overhead voltage, V_{OV}. The range is selected with the VOV bit (direct register 66, bit 4), and the value is selected with the VMIND register (indirect register 41). For revision B, V_{OV} is selected with the VOV bit (0 = 9V, 1 = 13.5V), and VMIND should be set to 6 decimal.
14. **Line Capacitance Compensation bits** – CLC bits in direct register 10 are functional in Revision E (and rev. D). They are not functional in revision B silicon.
15. **Daisy chain operation** – For revision E (and rev. D), daisy chain mode works properly regardless of the state of the SPIM bit (direct register 0, bit 6). For revision B, set SPIM=1 for daisy chain mode.

Si3210 Revision E (and rev. D) Registers

The added functionality of revision E (and rev. D) described above results in additional registers that are not defined in revision B. The specific function of each register is defined in the datasheet. The new registers for revision E/D are listed below.

Register Location	Register Description
Direct Register 52	FSK Data
Direct Register 63	Loop Closure Debounce for Automatic Ringing Cadence
Direct Register 108	Enhancement Enable
Indirect Register 43	Loop Closure Threshold—Lower Bound