

Silicon PNP Power Transistors

2SB834

DESCRIPTION

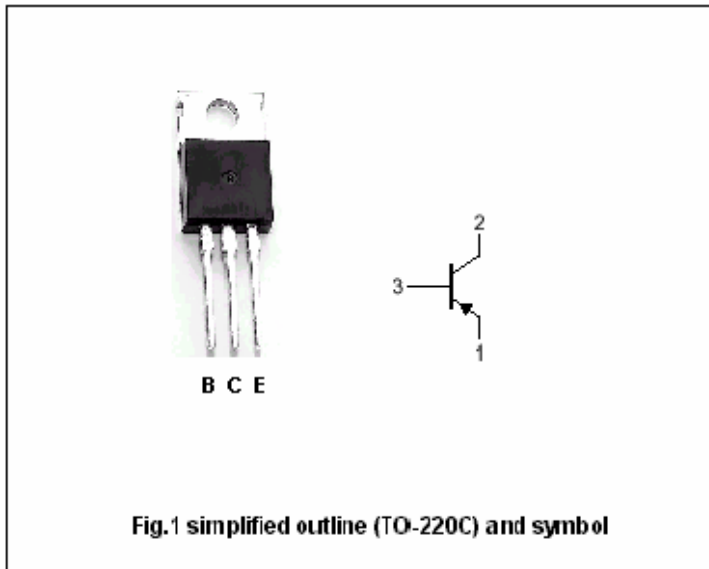
- With TO-220 package
- Low collector saturation voltage
- Complement to type 2SD880

APPLICATIONS

- Audio frequency power amplifier

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base



Absolute maximum ratings (Ta=25℃)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-60	V
V _{CEO}	Collector-emitter voltage	Open base	-60	V
V _{EBO}	Emitter-base voltage	Open collector	-7	V
I _C	Collector current		-3	A
I _B	Base current		-0.5	A
P _C	Collector power dissipation	T _a =25℃	1.5	W
		T _C =25℃	30	
T _j	Junction temperature		150	℃
T _{stg}	Storage temperature		-55~150	℃

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-50mA; I _B =0	-60			V
V _{BE}	Base-emitter on voltage	I _C =-0.5A; V _{CE} =-5V		-0.7	-1.0	V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-3A; I _B =-0.3A		-0.5	-1.0	V
I _{CBO}	Collector cut-off current	V _{CB} =-60V; I _E =0			-0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =-7V; I _C =0			-0.1	mA
h _{FE-1}	DC current gain	I _C =-0.5A; V _{CE} =-5V	60		200	
h _{FE-2}	DC current gain	I _C =-3A; V _{CE} =-5V	20			
C _{ob}	Collector output capacitance	I _E =0; V _{CB} =-10V; f=1MHz		150		pF
f _T	Transition frequency	I _C =-0.5A; V _{CE} =-5V		9		MHz

Switching times

t _{on}	Turn-on time	V _{CC} =-30V; R _L =15Ω I _{B1} =-I _{B2} =-0.2A		0.4		μs
t _s	Storage time			1.7		μs
t _f	Fall time			0.5		μs

◆ h_{FE-1} classifications

O	Y
60-120	100-200

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PACKAGE OUTLINE

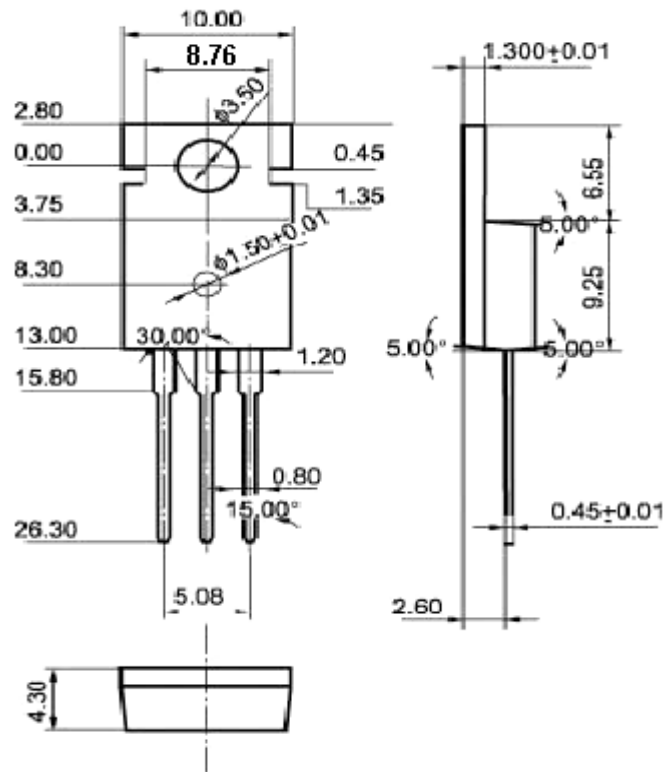


Fig.2 outline dimensions (unindicated tolerance: ± 0.10 mm)

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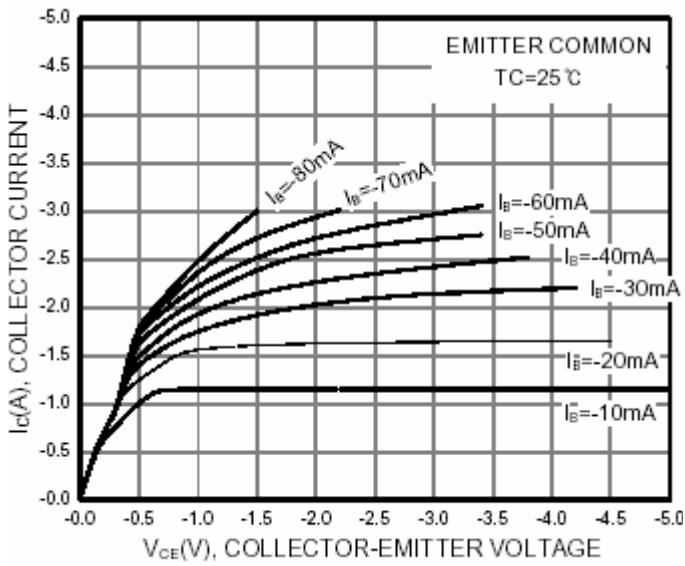


Fig.3 Static Characteristic

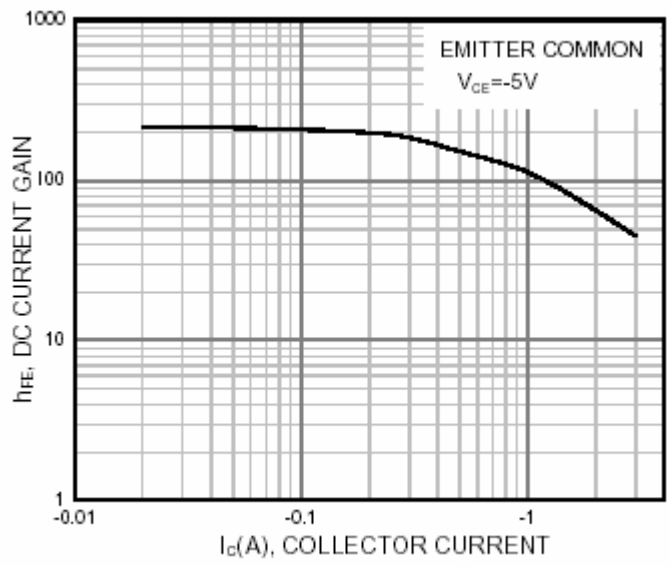


Fig.4 DC current Gain

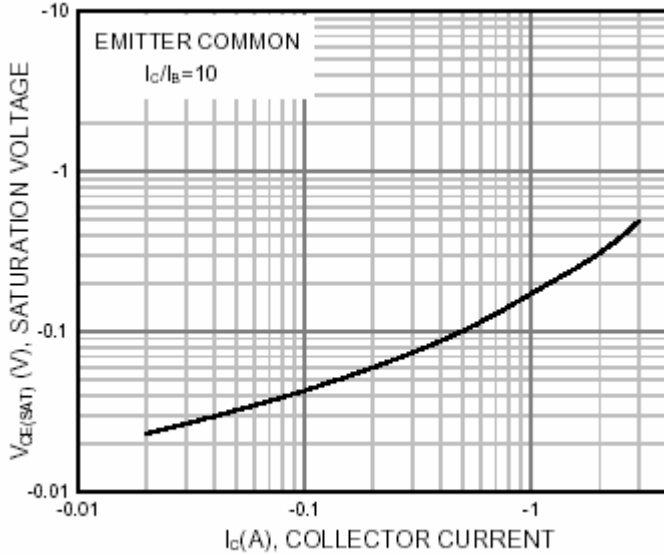


Fig.5 Collector-Emitter Saturation Voltage

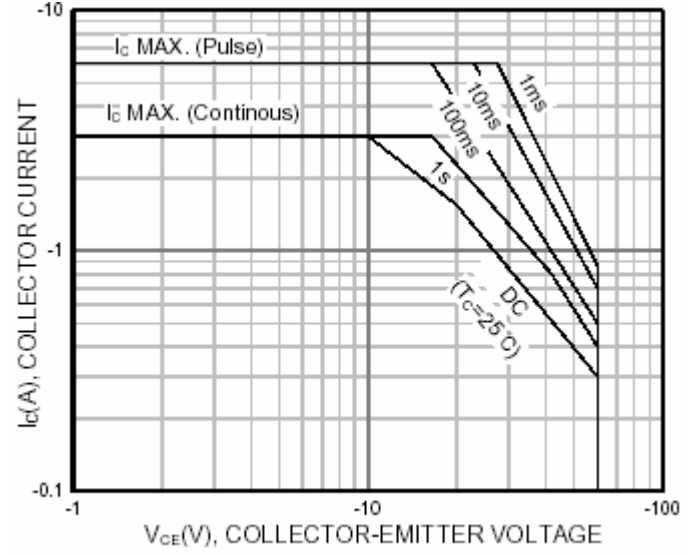


Fig.6 Safe Operating Area

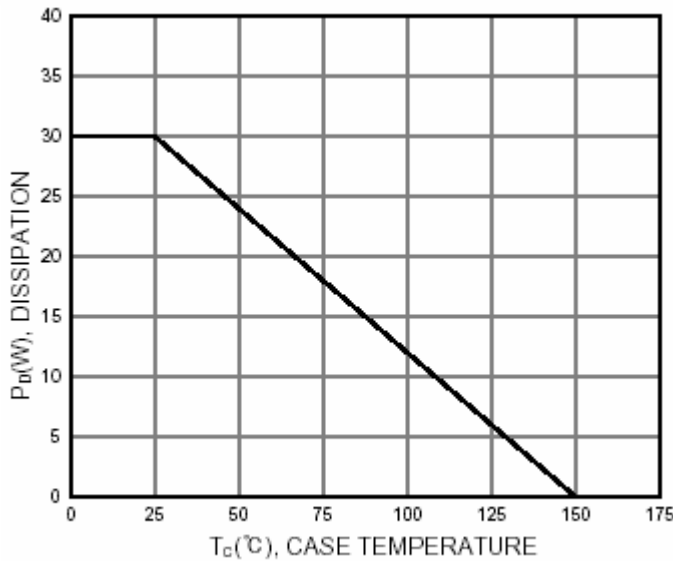


Fig.7 Power Derating