M48T86

5V PC REAL TIME CLOCK

- DROP-IN REPLACEMENT for PC COMPUTER CLOCK/CALENDAR
- COUNTS SECONDS, MINUTES, HOURS, DAYS, DAY of the WEEK, DATE, MONTH and YEAR with LEAP YEAR COMPENSATION
- INTERFACED WITH SOFTWARE AS 128 RAM LOCATIONS:
  - 14 Bytes of Clock and Control Registers
  - 114 Bytes of General Purpose RAM
- SELECTABLE BUS TIMING (Intel/Motorola)
- THREE INTERRUPTS are SEPARATELY SOFTWARE-MASKABLE and TESTABLE
  - Time-of-Day Alarm (Once/Second to Once/Day)
  - Periodic Rates from 122µs to 500ms
  - End-of-Clock Update Cycle
- PROGRAMMABLE SQUARE WAVE OUTPUT
- SELF-CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- PACKAGING INCLUDES a 28-LEAD SOIC and SNAPHAT® TOP (to be Ordered Separately)
- SOIC PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT TOP CONTAINS the BATTERY and CRYSTAL
- PIN and FUNCTION COMPATIBLE with bq3285/7A and DS128887

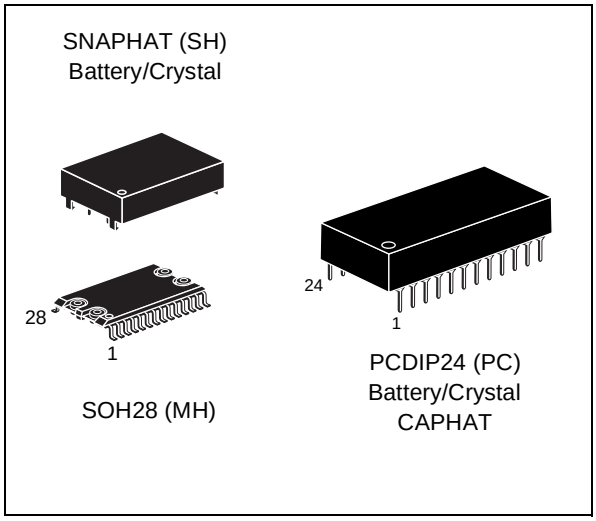


Figure 1. Logic Diagram

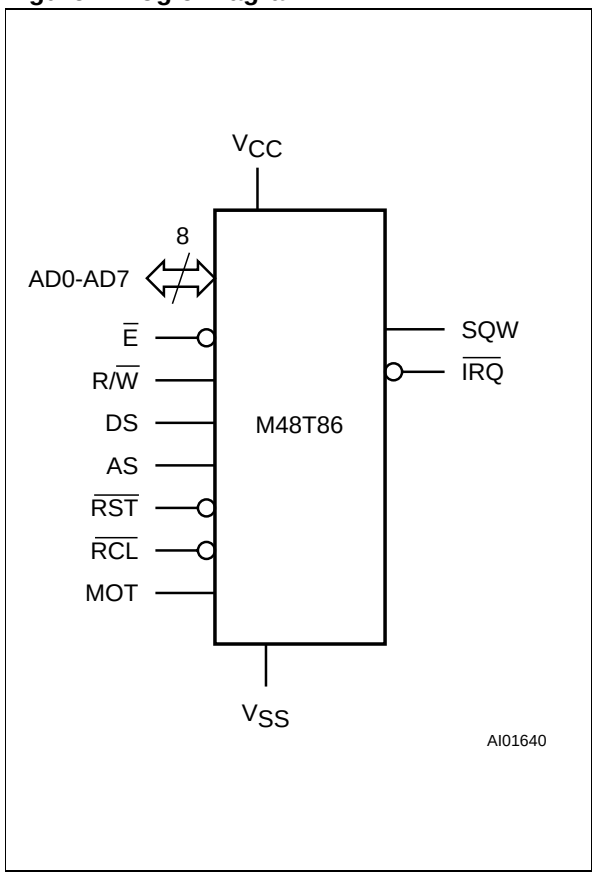


Figure 2. DIP Connections

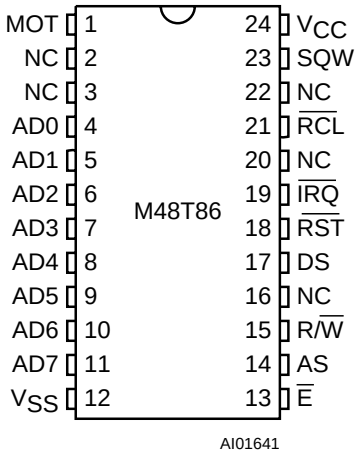


Figure 3. SOIC Connections

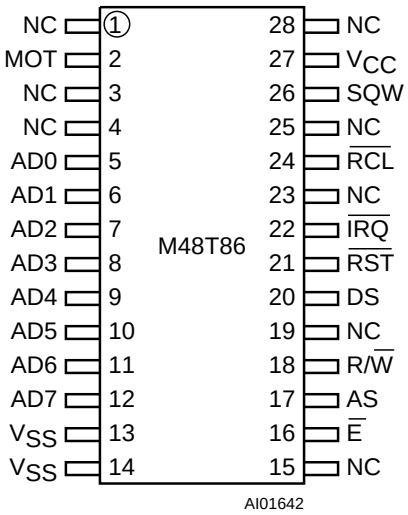


Table 1. Signal Names

AD0-AD7	Multiplexed Address/Data Bus
$\overline{E}$	Chip Enable Input
R/$\overline{W}$	Write Enable Input
DS	Data Strobe Input
AS	Address Strobe Input
$\overline{RST}$	Reset Input
$\overline{RCL}$	RAM Clear Input
MOT	Bus Type Select Input
SQW	Square Wave Output
$\overline{IRQ}$	Interrupt Request Output
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

DESCRIPTION

The M48T86 is an industry standard real time clock (RTC).The M48T86 is composed of a lithium energy source, quartz crystal, write-protection circuitry, and a 128 byte RAM array. This provides the user with a complete subsystem packaged in either a 24-pin DIP CAPHAT or 28-pin SNAPHAT SOIC. Functions available to the user include a non-volatile time-of-day clock, alarm interrupts, a one-hundred-year clock with programmable interrupts, square wave output, and 128 bytes of non-volatile static RAM.

The 24 pin 600mil DIP CAPHAT™ houses the M48T86 silicon with a quartz crystal and a long life lithium button cell in a single package.

The 28 pin 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SOIC and battery packages are shipped separately in plastic anti-static tubes or in Tape & Reel form.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
T_{SLD} (2)	Lead Solder Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7.0	V
V_{CC}	Supply Voltage	–0.3 to 7.0	V
P_D	Power Dissipation	1	W

Note: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

2. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

CAUTION: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

CAUTION: *Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.*

For the 28 lead SOIC, the battery/crystal package part number is "M4T28-BR12SH1".

Automatic deselection of the device provides insurance that data integrity is not compromised should V_{CC} fall below specified Power-fail Deselect Voltage (V_{PFD}) levels. The automatic deselection of the device remains in effect upon power up for a period of 200ms (max) after V_{CC} rises above V_{PFD}, provided that the Real Time Clock is running and the count down chain is not reset. This allows sufficient time for V_{CC} to stabilize and gives the system clock a wake up period so that a valid system reset can be established.

The block diagram in Figure 3 shows the pin connections and the major internal functions of the M48T86.

SIGNAL DESCRIPTION

V_{CC}, V_{SS}. DC power is provided to the device on these pins.The M48T86 utilizes a 5V V_{CC}.

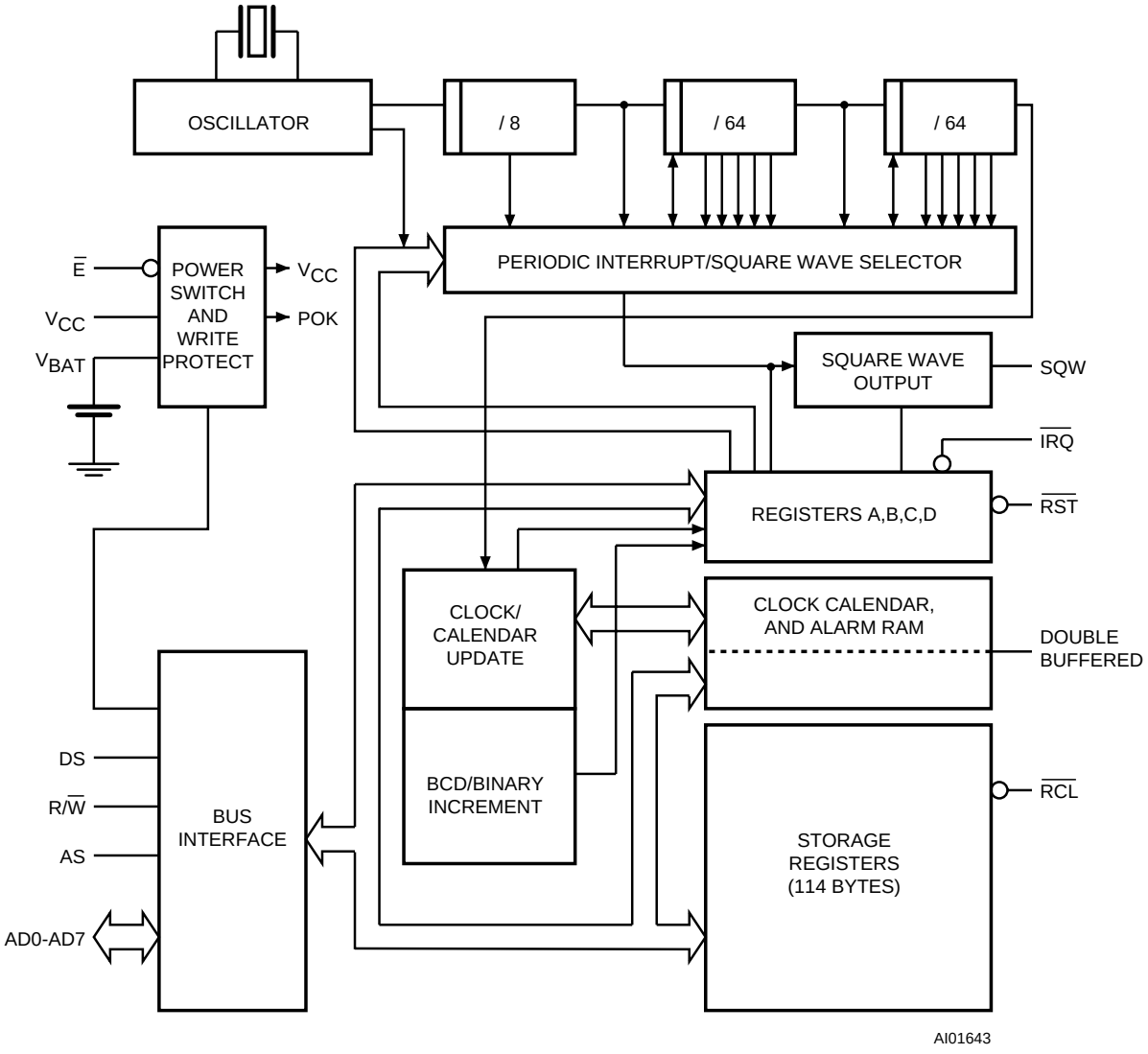
SQW (Square Wave Output). During normal operation (i.e. valid V_{CC}), the SQW pin can output a signal from one of 13 taps.The frequency of the SQW pin can be changed by programming Register A as shown in Table 10. The SQW signal can be turned on and off using the SQWE bit (Register B; bit 3). The SQW signal is not available when V_{CC} is less than V_{PFD}.

AD0-AD7 (Multiplexed Bi-Directional Address/ Data Bus). The M48T86 provides a multiplexed bus in which address and data information share the same signal path. The bus cycle consists of two stages; first the address is latched, followed by the data. Address/Data multiplexing does not slow the access time of the M48T86, since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS, at which time the M48T86 latches the address present on AD0-AD7. Valid write data must be present and held stable during the latter portion of the R/$\overline{W}$ pulse. In a read cycle, the M48T86 outputs 8 bits of data during the latter portion of the DS pulse. The read cycle is terminated and the bus returns to a high impedance state upon a high transition on R/$\overline{W}$.

AS (Address Strobe Input). A positive going pulse on the Address Strobe (AS) input serves to demultiplex the bus. The falling edge of AS causes the address present on AD0-AD7 to be latched within the M48T86.

MOT (Mode Select). The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to V_{SS} or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20K ohms.

Figure 4. Block Diagram



DS (Data Strobe Input). The DS pin is also referred to as Read (RD). A falling edge transition on the Data Strobe (DS) input enables the output during a a read cycle. This is very similar to an Output Enable ($\overline{G}$) signal on other memory devices.

$\overline{E}$ (Chip Enable Input). The Chip Enable pin must be asserted low for a bus cycle in the M48T86 to be accessed. Bus cycles which take place without asserting $\overline{E}$ will latch the addresses present, but no data access will occur.

$\overline{IRQ}$ (Interrupt Request Output). The $\overline{IRQ}$ pin is an open drain output that can be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. $\overline{IRQ}$ returns to a high impedance state whenever Register C is read. The $\overline{RST}$ pin can also be used to clear pending interrupts. Because the $\overline{IRQ}$ bus is an open drain output, it requires an external pull-up resistor to V_{CC}.

$\overline{\text{RST}}$ (Reset Input). The M48T86 is reset when the $\overline{\text{RST}}$ input is pulled low. With a valid V_{CC} applied and a low on $\overline{\text{RST}}$, the following events occur:

1. Periodic Interrupt Enable (PIE) bit is cleared to a zero. (Register B; Bit 6)
2. Alarm Interrupt Enable (AIE) bit is cleared to a zero.(Register B; bit 5)
3. Update Ended Interrupt Request (UF) bit is cleared to a zero. (Register C; Bit 4)
4. Interrupt Request (IRQF) bit is cleared to a zero. (Register C Bit 7)
5. Periodic Interrupt Flag (PF) bit is cleared to a zero. (Register C; Bit 6)
6. The device is not accessible until $\overline{\text{RST}}$ is returned high.
7. Alarm Interrupt Flag (AF) bit is cleared to a zero. (Register C; Bit 5)
8. The $\overline{\text{IRQ}}$ pin is in the high impedance state.
9. Square Wave Output Enable (SQWE) bit is cleared to zero. (Register B; Bit 3).
10. Update Ended Interrupt Enable (UIE) is cleared to a zero. (Register B; Bit 4)

$\overline{\text{RCL}}$ (RAM Clear). The $\overline{\text{RCL}}$ pin is used to clear all 114 storage bytes, excluding clock and control registers, of the array to FF(hex) value. The array will be cleared when the $\overline{\text{RCL}}$ pin is held low for at least 100ms with the oscillator running. Usage of this pin does not affect battery load. This function is applicable only when V_{CC} is applied.

R/$\overline{\text{W}}$ (Read/Write Input). The R/$\overline{\text{W}}$ pin is utilized to latch data into the M48T86 and provides functionality similar to $\overline{\text{W}}$ in other memory systems.

ADDRESS MAP

The address map of the M48T86 is shown in Figure 9. It consists of 114 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar and alarm data, and 4 bytes which are used for control and status. All bytes can be read or written to except for the following:

1. Registers C & D are read-only.
2. Bit 7 of Register A is read-only.

The contents of the four Registers A, B, C, and D are described in the "Registers" section.

Table 3. Time, Calendar and Alarm Formats

Address	RTC Bytes	Range		
		Decimal	Binary	BCD
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours, 12-hrs	1-12	01-0C AM 81-8C PM	01-12 AM 81-92 PM
	Hours, 24-hrs	0-23	00-17	00-23
5	Hours Alarm, 12-hrs	1-12	01-0C AM 81-8C PM	01-12 AM 81-92 PM
	Hours Alarm, 24-hrs	0-23	00-17	00-23
6	Day of Week (1 = Sun)	1-7	01-07	01-07
7	Day of Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

TIME, CALENDAR, AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, and alarm registers are set or initialized by writing the appropriate RAM bytes. The contents of the time, calendar, and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm register, the SET bit (Register B; Bit 7) should be written to a logic "1". This will prevent updates from occurring while access is being attempted. In addition to writing the time, calendar, and alarm registers in a selected format (binary or BCD), the Data Mode (DM) bit (Register B; Bit 2), must be set to the appropriate logic level ("1" signifies binary data; "0" signifies Binary Coded Decimal (BCD data). All time, calendar, and alarm bytes must use the same data mode. The SET bit should be cleared after the Data Mode bit has been written to allow the Real Time Clock to update the time and calendar bytes. Once initialized, the Real Time Clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 3 shows the binary and BCD formats of the time, calendar, and alarm locations. The 24/12 bit (Register B; Bit 1) cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, a logic one in the high order bit of the hours byte represents PM. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. However, the probability of reading incorrect time and calendar data is low. Methods of avoiding possible incorrect time and calendar reads are reviewed later in this text.

NON-VOLATILE RAM

The 114 general purpose non-volatile RAM bytes are not dedicated to any special function within the M48T86. They can be used by the processor program as non-volatile memory and are fully accessible during the update cycle.

Figure 5. AC Testing Load Circuit

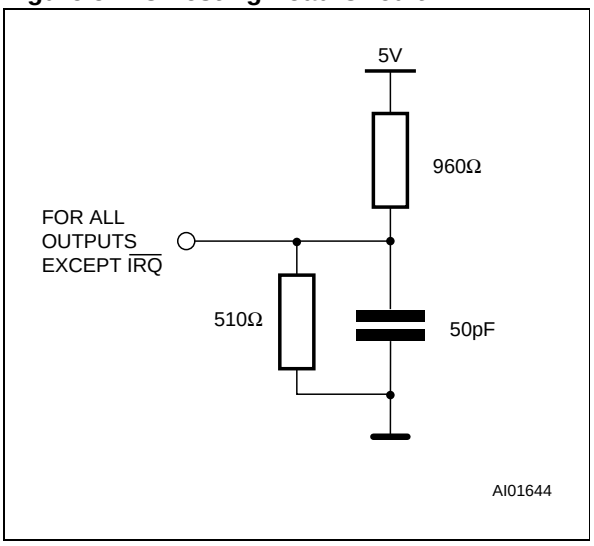


Figure 6. AC Testing Load Circuit

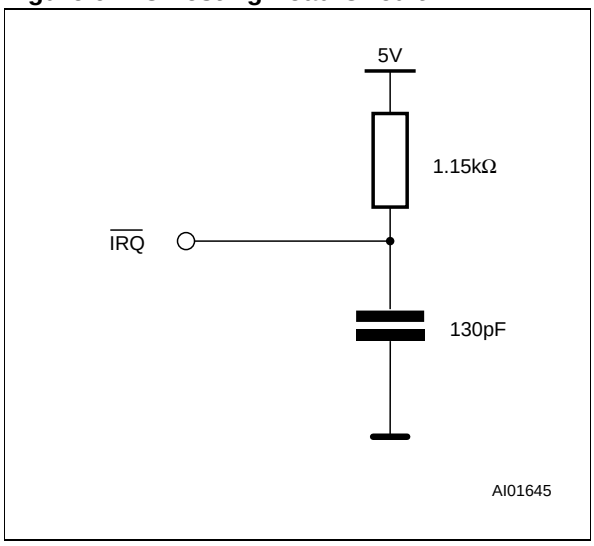


Table 4. AC Measurement Conditions

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Table 5. Capacitance (1, 2)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		7	pF
C_{IO} (3)	Input / Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected.

Table 6. DC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±1	µA
I_{CC}	Supply Current	Outputs open		15	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA		0.4	V
	Output Low Voltage ($\overline{IRQ}$)	I_{OL} = 0.5mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 7. Power Down/Up Trip Points DC Characteristics (1)
(T_A = 0 to 70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage	4.0		4.35	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} (2)	Expected Data Retention Time	10			YEARS

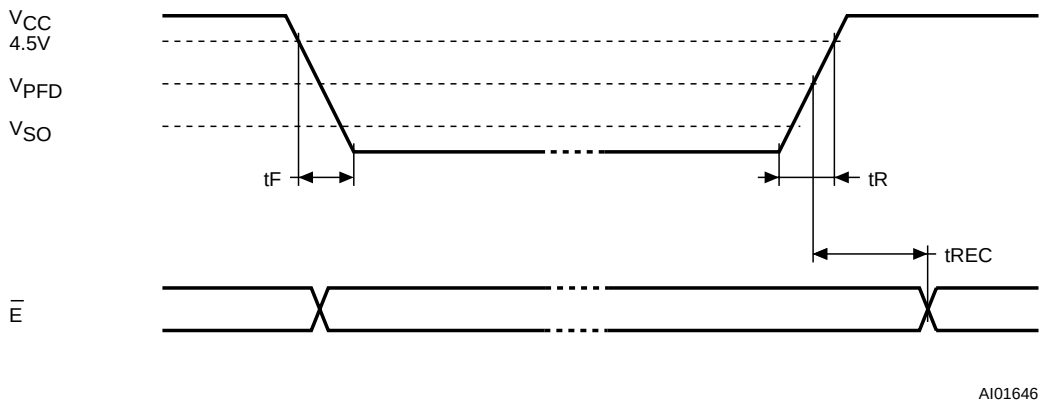
Note: 1. All voltages referenced to V_{SS}.
2. At 25°C.

Table 8. Power Down/Up Mode AC Characteristics
(TA = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{CC} Fall Time	300		µs
t_R	V_{CC} Rise Time	100		µs
t_{REC}	V_{PFD} to $\overline{E}$ High	20	200	ms

Note: 1. V_{CC} fall time of less than t_F may result in deselection/write protection not occurring until 200µs after V_{CC} passes V_{PFD}.

Figure 7. Power Down/Up Mode AC Waveforms



INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt (alarm, periodic, update-in-progress) available to a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected from rates of 500ms to 122µs. The update-ended interrupt can be used to indicate that an update cycle has completed.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic "1" to an interrupt-enable bit (Register B; Bit 6 = PIE; Bit 5 = AIE; Bit 4 = UIE) permits an interrupt to be initialized when the event occurs. A zero in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

Table 9. AC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	M48T86			Unit
		Min	Typ	Max	
t_{CYC}	Cycle Time	160			ns
t_{DSL}	Pulse Width, Data Strobe Low or R/$\overline{W}$ High	80			ns
t_{DSH}	Pulse Width, Data Strobe High or R/$\overline{W}$ Low	55			ns
t_{RWH}	R/$\overline{W}$ Hold Time	0			ns
t_{RWS}	R/$\overline{W}$ Setup Time	10			ns
t_{CS}	Chip Select Setup Time	5			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{DHR}	Read Data Hold Time	0		25	ns
t_{DHW}	Write Data Hold Time	0			ns
t_{AS}	Address Setup Time	20			ns
t_{AH}	Address Hold Time	5			ns
t_{DAS}	Delay Time, Data Strobe to Address Strobe Rise	10			ns
t_{ASW}	Pulse Width Address Strobe High	30			ns
t_{ASD}	Delay Time, Address Strobe to Data Strobe Rise	35			ns
t_{OD}	Output Data Delay Time from Data Strobe Rise			50	ns
t_{DW}	Write Setup Time	30			ns
t_{BUC}	Delay Time before Update Cycle		244		µs
t_{PI} (1)	Periodic Interrupt Time interval	–	–	–	
t_{UC}	Time of Update Cycle		1		µs

Note: 1. See Table 10.

When an interrupt event occurs, the related flag bit (Register C; Bit 6 = PF; Bit 5 = AF; Bit 4 = UF) is set to a logic "1". These flag bits are set independent of the state of the corresponding enable bit in Register B and can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bits are status bits which software can interrogate as necessary.

When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as all are cleared each time Register C is read. Double latching is included with Register C so that bits which are set, remain stable throughout the read cycle. All bits which are set high are cleared when read. Any new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The $\overline{IRQF}$ bit (Register C; Bit 7) is a "1" whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C.A logic "1" in the IRQF bit indicates that one or more interrupts have been initiated by the M48T86. The act of reading Register C clears all active flag bits and the IRQF bit.

Figure 8. Intel Bus Read Mode AC Waveforms

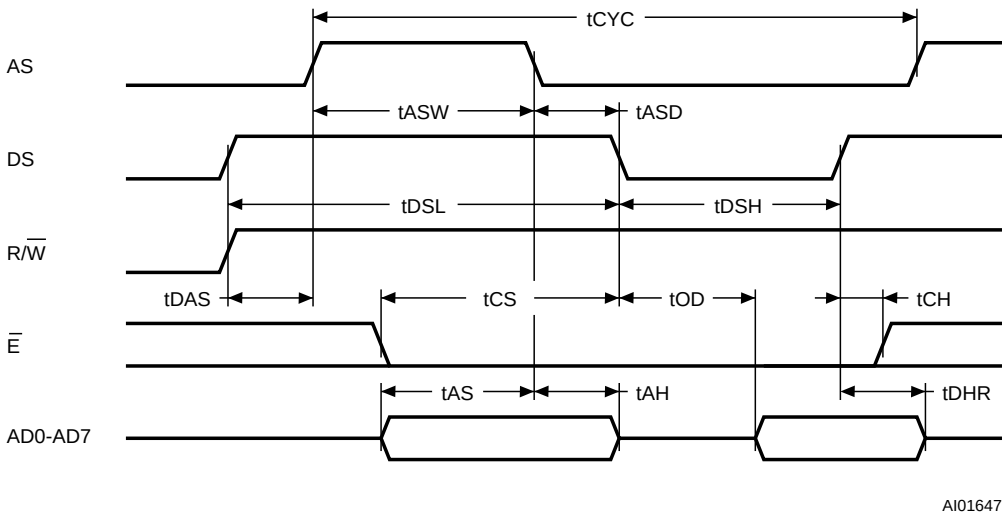


Figure 9. Intel Bus Write AC Waveforms

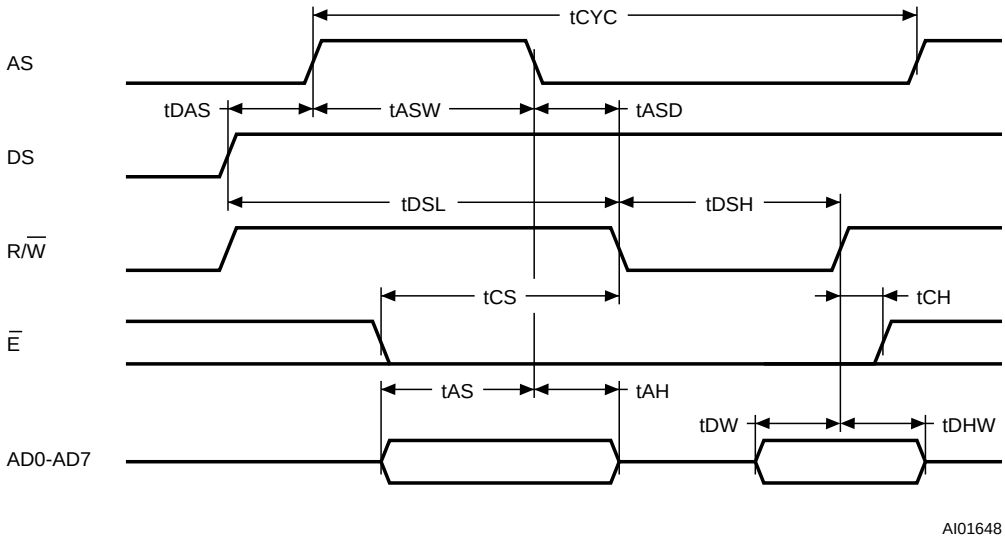
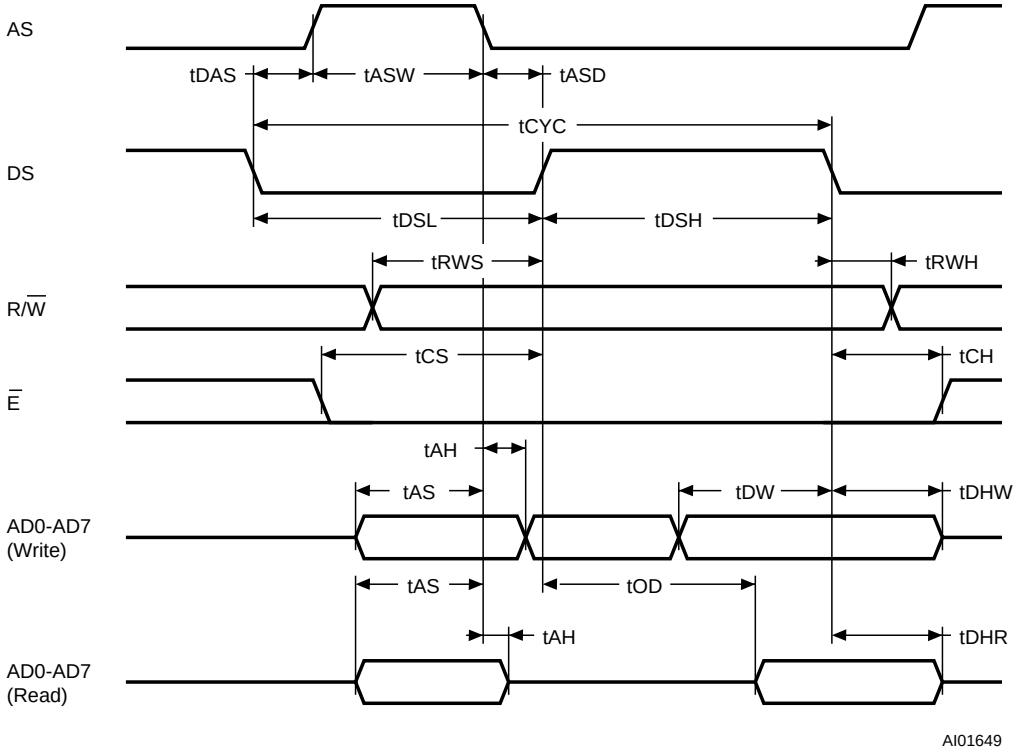


Figure 10. Motorola Bus Read/Write Mode AC Waveforms



PERIODIC INTERRUPT

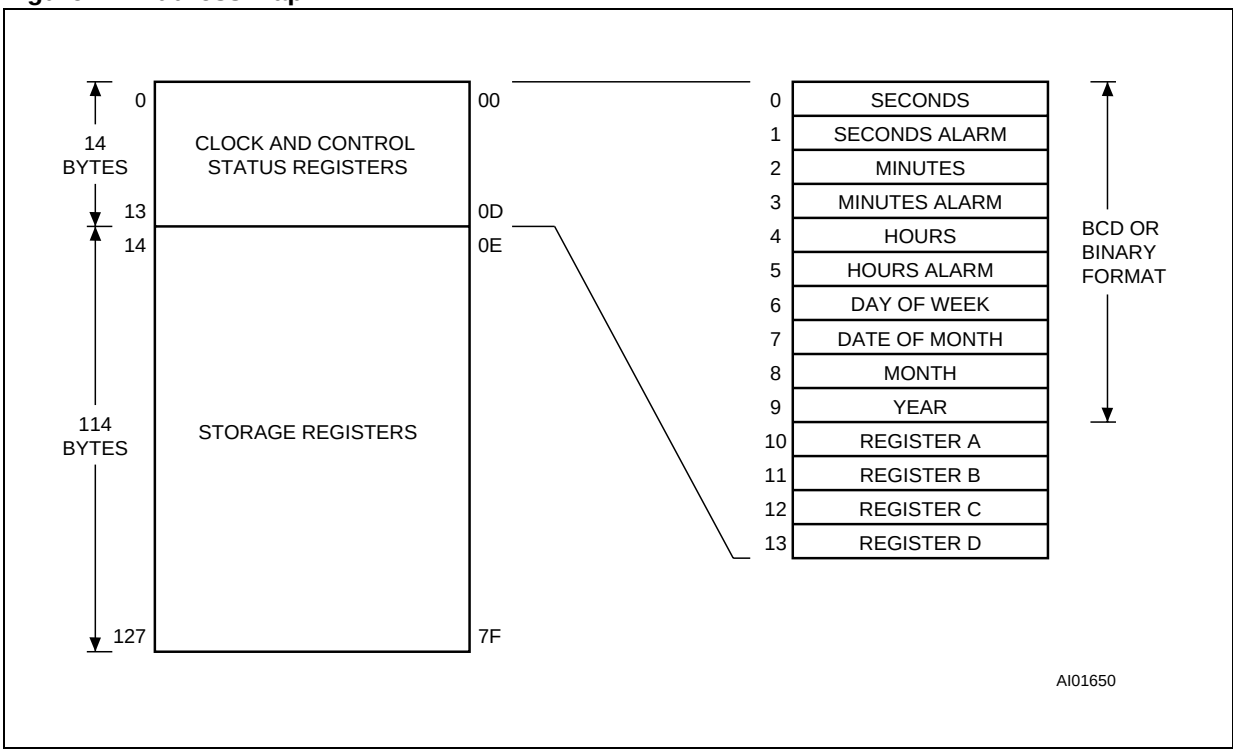
The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500ms to once every 122µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 10). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The periodic interrupt is enabled by the PIE bit (Register B; Bit 6). The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

ALARM INTERRUPT

The alarm interrupt provides the system processor with an interrupt when a match is made between the RTC's hours, minutes, and seconds bytes and the corresponding alarm bytes.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the Alarm Interrupt Enable bit (Register B; Bit 5) is high. The second use is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic "1". An alarm will be generated each hour when the "don't care" is are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hour and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Figure 11. Address Map



UPDATE CYCLE INTERRUPT

After each update cycle, the update cycle ended flag bit (UF) (Register C; Bit 4) is set to a "1". If the update interrupt enable bit (UIE) (Register B; Bit 4) is set to a "1", and the SET bit (Register B; Bit 7) is a "0", then an interrupt request is generated at the end of each update cycle.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 3. The purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS3-RS0 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 10. The SQW frequency selection shares the 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enabled (SQWE).

OSCILLATOR CONTROL BITS

When the M48T86 is shipped from the factory the internal oscillator is turned off. This feature prevents the lithium energy cell from being discharged until it is installed in a system. A pattern of "010" in Bits 4-6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of "11X" will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of Bits 4-6 keep the oscillator off.

Table 10. Square Wave Frequency/Periodic Interrupt Rate

Register A Bits				Square Wave		Periodic Interrupt	
RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	0	0	0	None		None	
0	0	0	1	256	Hz	3.90625	ms
0	0	1	0	128	Hz	7.8125	ms
0	0	1	1	8.192	kHz	122.070	us
0	1	0	0	4.096	kHz	244.141	us
0	1	0	1	2.048	kHz	488.281	us
0	1	1	0	1.024	kHz	976.5625	us
0	1	1	1	512	Hz	1.953125	ms
1	0	0	0	256	Hz	3.90625	ms
1	0	0	1	128	Hz	7.8125	ms
1	0	1	0	64	Hz	15.625	ms
1	0	1	1	32	Hz	31.25	ms
1	1	0	0	16	Hz	62.5	ms
1	1	0	1	8	Hz	125	ms
1	1	1	0	4	Hz	250	ms
1	1	1	1	2	Hz	500	ms

UPDATE CYCLE

The M48T86 executes an update cycle once per second regardless of the SET bit (Register B; Bit 7). When the SET bit is asserted, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows accurate time to be maintained, independent of reading and writing the time, calendar, and alarm buffers. This also guarantees that the time and calendar information will be consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods of accessing the real time clock that will avoid any possibility of obtaining inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999ms are available to read valid time and date information. If this interrupt is used, the IRQF bit (Register C; Bit 7) should be cleared before leaving the interrupt routine.

A second method uses the Update-In-Progress (UIP) bit (Register A; Bit 7) to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244µs later. If a low is read on the UIP bit, the user has at least 244µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit is set high between the setting of the PF bit (Register C; Bit 6). Periodic interrupts that occur at a rate greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt.The reads should be completed within $1/(t_{PL/2} + t_{BUC})$ to ensure that data is not read during the update cycle.

Figure 12. Update Period Timing and UIP

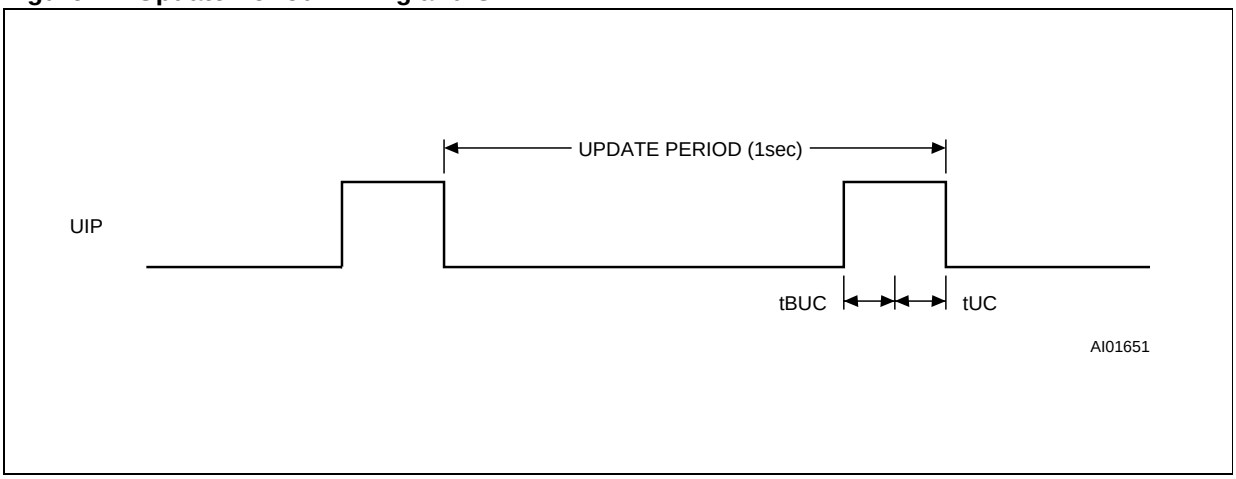
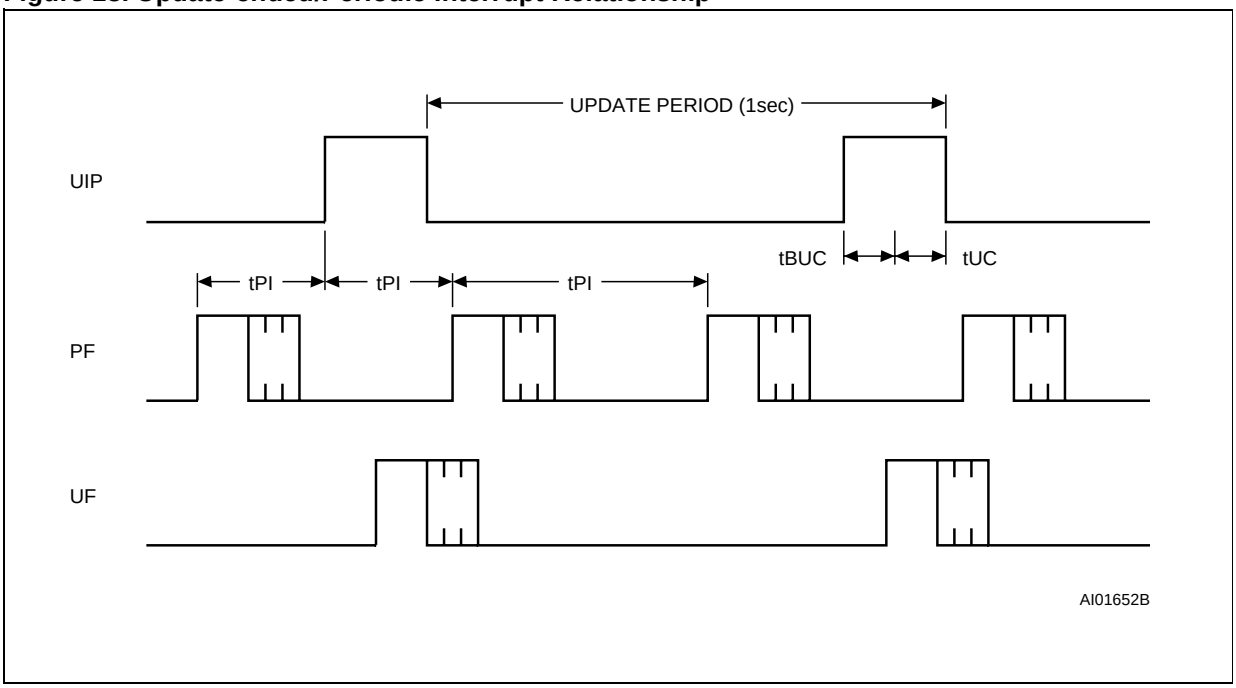


Figure 13. Update-ended/Periodic Interrupt Relationship



REGISTER A

MSB

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
UIP	OSC2	OSC1	OSC0	RS3	RS2	RS1	RS0

UIP. Update in Progress

The Update in Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is one, the update transfer will soon occur. When UIP isa zero, the update transfer will not occur for at least 244µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by RST. Writing the SET bit in Register B to a "1" inhibits any update transfer and clears the UIP status bit.

OSC0, OSC1, OSC2. Oscillator Control

These three bits are used to control the oscillator and reset the countdown chain. A pattern of "010" enables operation by turning on the oscillator and enabling the divider chain. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When "010" is written, the first update begins after 500ms.

RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user may do one of the following:

1. Enable the interrupt with the PIE bit;

or

2. Enable the SQW output with the SQWE bit;

or

3. Enable both at the same time and same rate;

or

4. Enable neither.

Table 10 lists the periodic interrupt rates and the square wave frequencies that may be chosen with the RS bits. These four read/write bits are not affected by RST.

REGISTER B

MSB

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET

When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program may initialize the time and calendar bytes without an update occurring. Read cycles can be executed in a similar manner. SET is a read/write bit which is not modified by $\overline{RST}$ or internal functions of the M48T86.

PIE. Periodic Interrupt Enable

The Periodic Interrupt Enable bit (PIE) is a read/write bit which allows the Periodic Interrupt Flag (PF) bit Register C to cause the $\overline{IRQ}$ pin to be driven low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal M48T86 functions, but is cleared to zero on $\overline{RST}$.

AIE. Alarm Interrupt Enable

The Alarm Interrupt Enable (AIE) bit is a Read/Write bit which, when set to a one, permits the Alarm Flag (AF) bit in Register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 1XXXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The $\overline{RST}$ pin clears AIE to zero. The internal functions of the M48T86 do not affect the AIE bit.

UIE. Update Ended Interrupt Enable

The Update Ended Interrupt Enable (UIE) bit is a read/write bit which enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. A transition low on the $\overline{RST}$ pin or the SET bit going high clears the UIE bit.

SQWE. Square Wave Enable

When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal is driven out on the SQW pin. The frequency is determined by the rate-selection bits RS3-RS0. When the SQWE bit is set to zero, the SQW pin is held low. The SQWE bit is cleared by the $\overline{RST}$ pin. SQWE is a read/write bit.

DM. Data Mode

The Data Mode (DM) bit indicates whether time and calendar information are in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal function or $\overline{RST}$. A one in DM signifies binary data and a zero specifies Binary Coded Decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours byte.A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write and is not affected by internal functions or $\overline{RST}$.

DSE. Daylight Savings Enable

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when set to a one. On the first Sunday in April, the time increments from 1:59:59AM to 3:00:00 AM. On the last Sunday in October, when the time reaches 1:59:59 AM, it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or $\overline{RST}$.

REGISTER C

MSB

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IRQF	PF	AF	UF	0	0	0	0

IRQF. Interrupt Request Flag

The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1

AF = AIE = 1

UF = UIE = 1

(i.e. IRQF = PF*PIE+AF*AIE+UF*UIE)

PF. Periodic Interrupt Flag

The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3-RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. The $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{RST}$ or a software read of Register C.

AF. Alarm Flag

A one in the AF (Alarm Interrupt Flag) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A $\overline{RST}$ or a read of Register C will clear AF.

UF. Update Ended Interrupt Flag

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to a one, the one in the UF bit causes the IRQF bit to be a one. This will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C or an $\overline{RST}$.

BIT 0 through 3. Unused Bits

Bit 3-Bit 0 are unused. These bits always read zero and cannot be written.

REGISTER D

MSB

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VRT	0	0	0	0	0	0	0

VRT. Valid Ram And Time

The Valid RAM and Time (VRT) bit is set to the one state by STMicroelectronics prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium cell is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{RST}$.

BIT 0 through 6. Unused Bits

The remaining bits of Register D are not usable. They cannot be written and when read, they will always read zero.

POWER SUPPLY DECOUPLING and UNDERSHOOT PROTECTION

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (as shown in Figure 14) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one Volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 14. Supply Voltage Protection

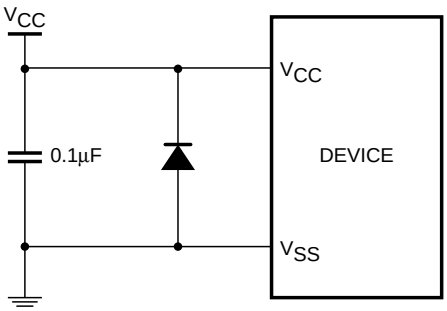


Table 11. Ordering Information Scheme

Example: M48T86 MH 1 TR

Device Type
M48T

Package
PC = PCDIP24
MH (1) = SOH28

Temperature Range
1 = 0 to 70 °C

Shipping Method for SOIC
blank = Tubes
TR = Tape & Reel

Note: 1. The SOIC package (SOH28) requires the battery/crystal package (SNAPHAT) which is ordered separately under the part number "M4T28-BR12SH1" in plastic tube or "M4T28-BR12SH1TR" in Tape & Reel form.

Caution: Do not place the SNAPHAT battery/crystal package "M4T28-BR12SH1" in conductive foam since will drain the lithium button-cell battery.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

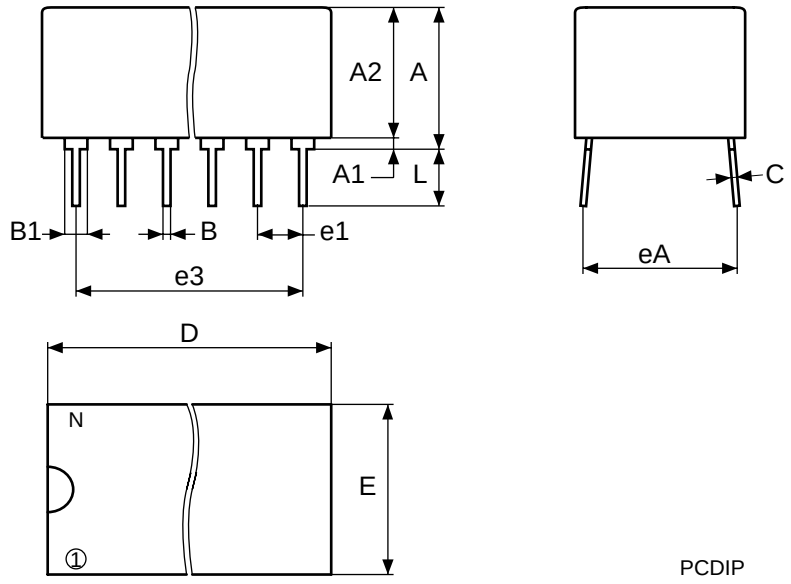
Table 12. Revision History

Date	Revision Details
March 1999	First Issue
05/04/00	Page layout changed

Table 13. PCDIP24 - 24 pin Plastic DIP, battery CAPHAT, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.3500	0.3799
A1		0.38	0.76		0.0150	0.0299
A2		8.36	8.89		0.3291	0.3500
B		0.38	053		0.0150	0.0209
B1		1.14	1.78		0.0449	0.0701
C		0.20	0.31		0.0079	0.0122
D		34.29	34.80		1.3500	1.3701
E		17.83	18.34		0.7020	0.7220
e1		2.29	2.79		0.0902	0.1098
e3		25.15	30.73		0.9902	1.2098
eA		15.24	16.00		0.6000	0.6299
L		3.05	3.81		0.1201	0.1500
N	24			24		

Figure 15. PCDIP28 - 28 pin Plastic DIP, battery CAPHAT, Package Outline

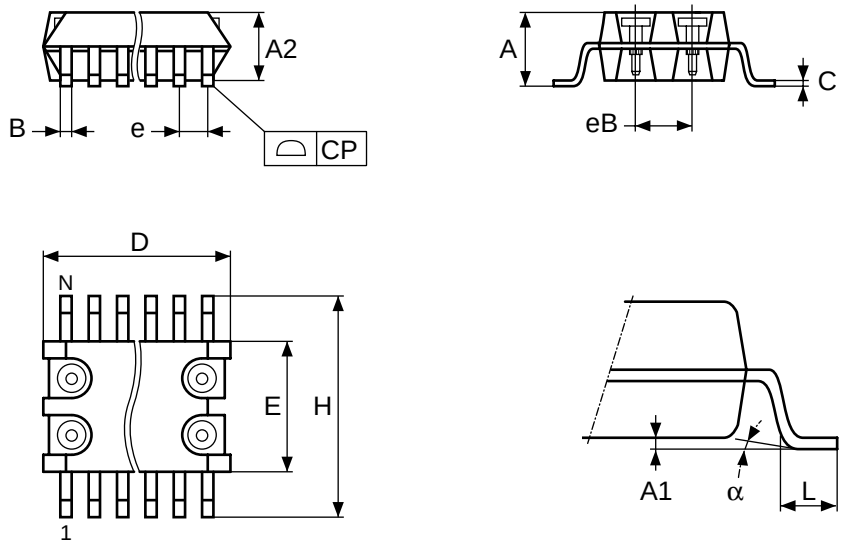


Drawing is not to scale.

Table 14. SOH28 - 28 lead Plastic Small Outline, 4-socket battery SNAPHAT, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.1201
A1		0.05	0.36		0.0020	0.0142
A2		2.34	2.69		0.0921	0.1059
B		0.36	0.51		0.0142	0.0201
C		0.15	0.32		0.0059	0.0126
D		17.71	18.49		0.6972	0.7280
E		8.23	8.89		0.3240	0.3500
e	1.27	–	–	0.0500	–	–
eB		3.20	3.61		0.1260	0.1421
H		11.51	12.70		0.4531	0.5000
L		0.41	1.27		0.0161	0.0500
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.0039

Figure 16. SOH28 - 28 lead Plastic Small Outline, 4-socket battery SNAPHAT, Package Outline



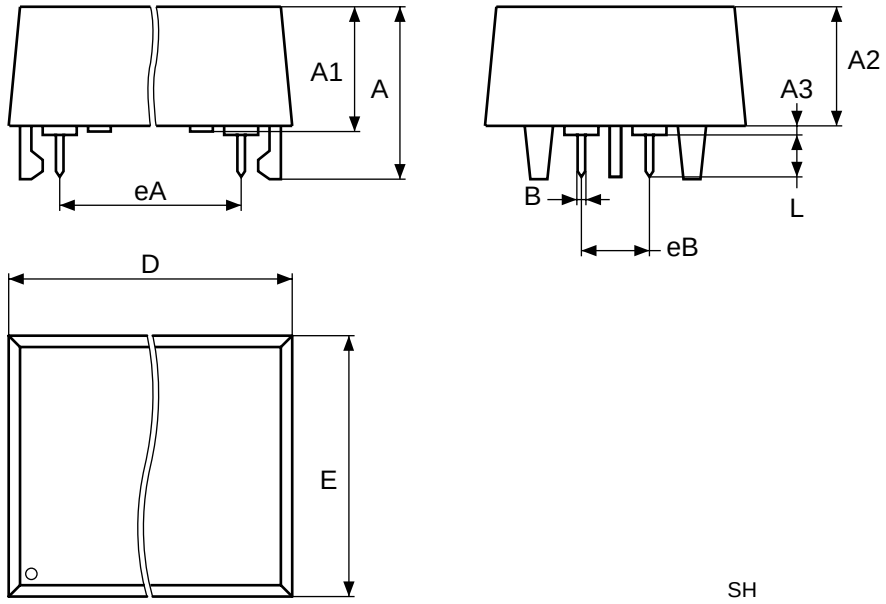
SOH-A

Drawing is not to scale.

Table 15. M4T28-BR12SH - SNAPHAT Housing for 48 mAh Battery & Crystal, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.3850
A1		6.73	7.24		0.2650	0.2850
A2		6.48	6.99		0.2551	0.2752
A3			0.38			0.0150
B		0.46	0.56		0.0181	0.0220
D		21.21	21.84		0.8350	0.8598
E		14.22	14.99		0.5598	0.5902
eA		15.55	15.95		0.6122	0.6280
eB		3.20	3.61		0.1260	0.1421
L		2.03	2.29		0.0799	0.0902

Figure 17. M4T28-BR12SH - SNAPHAT Housing for 48 mAh Battery & Crystal, Package Outline



Drawing is not to scale.