CS5525
CS5526

16-Bit/20-Bit Multi-Range ADC with 4-Bit Latch

Features

- Delta-Sigma A/D Converter
  - Linearity Error: 0.0015%FS
  - Noise Free Resolution: 18-bits
- Bipolar/Unipolar Input Ranges
  - 25 mV, 55 mV, 100 mV, 1 V, 2.5 V and 5 V
- Chopper Stabilized Instrumentation Amplifier
- On-Chip Charge Pump Drive Circuitry
- 4-Bit Output Latch
- Simple three-wire serial interface
  - SPI™ and Microwire™ Compatible
  - Schmitt Trigger on Serial Clock (SCLK)
- Programmable Output Word Rates
  - 3.76 Hz to 202Hz (XIN = 32.768 kHz)
  - 11.47 Hz to 616 Hz (XIN = 100 kHz)
- Output Settles in One Conversion Cycle
- Simultaneous 50/60 Hz Noise Rejection
- System and Self-Calibration with Read/Write Registers
- Single +5 V Analog Supply +3.0 V or +5 V Digital Supply
- Low Power Mode Consumption: 4.9 mW
  - 1.8 mW in 1 V, 2.5 V, and 5 V Input Ranges

General Description

The 16-bit CS5525 and the 20-bit CS5526 are highly integrated ΔΣ A/D converters which include an instrumentation amplifier, a PGA (programmable gain amplifier), eight digital filters, and self and system calibration circuitry.

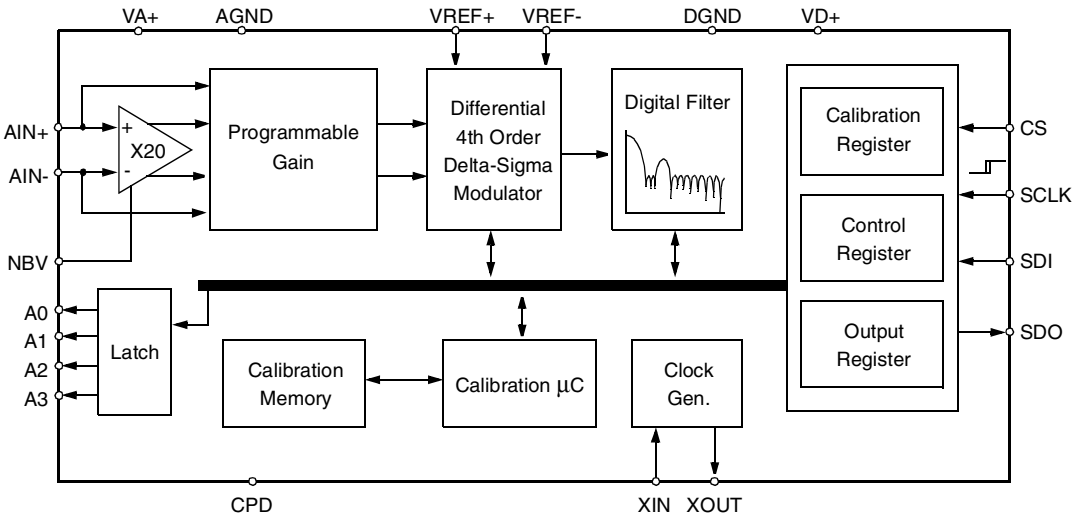
The converters are designed to provide their own negative supply which enables their on-chip instrumentation amplifiers to measure bipolar ground-referenced signals ≤±100 mV. By directly supplying NBV with -2.5 V and with VA+ at 5 V, ±2.5 V signals (with respect to ground) can be measured.

The digital filters provide programmable output update rates between 3.76 Hz to 202 Hz (XIN = 32.768 kHz). Output word rates can be increased by approximately 3X by using XIN = 100 kHz. Each filter is designed to settle to full accuracy for its output update rate in one conversion cycle. The filters with word rates of 15 Hz or less (XIN = 32.768 kHz) reject both 50 and 60 Hz (±3 Hz) line interference simultaneously.

Low power, single conversion settling time, programmable output rates, and the ability to handle negative input signals make these single supply products ideal solutions for isolated and non-isolated applications.

ORDERING INFORMATION

See page26.



ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5 V ±5%; VREF+ = 2.5 V, VREF- = AGND, NBV = -2.1 V, FCLK = 32.768 kHz, OWR (Output Word Rate) = 15 Hz, Bipolar Mode, Input Range = ±100 mV; See Notes 1 and 2.)

Parameter		CS5525 Min	CS5525 Typ	CS5525 Max	CS5526 Min	CS5526 Typ	CS5526 Max	Unit
Accuracy								
Linearity Error		-	±0.0015	±0.003	-	±0.0007	±0.0015	%FS
No Missing Codes		16	-	-	20	-	-	Bits
Bipolar Offset	(Note 3)	-	±1	±2	-	±16	±32	LSB
Unipolar Offset	(Note 3)	-	±2	±4	-	±32	±64	LSB
Offset Drift	(Notes 3 and 4)	-	20	-	-	20	-	nV/°C
Bipolar Gain Error		-	±8	±31	-	±8	±31	ppm
Unipolar Gain Error		-	±16	±62	-	±16	±62	ppm
Gain Drift	(Note 4)	-	1	3	-	1	3	ppm/°C
Voltage Reference Input								
Range	(VREF+) - (VREF-)	1	2.5	3.0	1	2.5	3.0	V
Common Mode Rejection	dc	-	110	-	-	110	-	dB
	50, 60 Hz	-	130	-	-	130	-	dB
Input Capacitance		-	16	-	-	16	-	pF
CVF Current	(Note 5)	-	0.6	-	-	0.6	-	µA/V

Notes:
1. Applies after system calibration at any temperature within -40 °C ~ +85 °C.
2. Specifications guaranteed by design, characterization, and/or test.
3. Specification applies to the device only and does not include any effects by external parasitic thermocouples. LSB = LSB_{16} for the CS5525, and LSB_{20} for the CS5526.
4. Drift over specified temperature range after calibration at power-up at 25 °C.
5. See the section of the data sheet which discusses input models on page 15.

RMS NOISE (Notes 6 and 7)

Output Rate (Hz)	-3 dB Filter Frequency	Input Range, (Bipolar/Unipolar Mode) 25 mV	55 mV	100 mV	1 V	2.5 V	5 V
3.76	3.27	90 nV	90 nV	130 nV	1.0 µV	2.0 µV	4.0 µV
7.51	6.55	110 nV	130 nV	190 nV	1.5 µV	3.0 µV	7 µV
15.0	12.7	170 nV	200 nV	250 nV	2.0 µV	5.0 µV	10 µV
30.1	25.4	250 nV	300 nV	500 nV	4.0 µV	10 µV	15 µV
60.0	50.4	500 nV	1.0 µV	1.5 µV	15 µV	45 µV	85 µV
123.2 (Note 8)	103.6	2.0 µV	4.0 µV	8.0 µV	72 µV	190 µV	350 µV
168.9 (Note 8)	141.3	10 µV	20.0 µV	30 µV	340 µV	900 µV	2.0 mV
202.3 (Note 8)	169.2	30 µV	55 µV	105 µV	1.1 mV	2.4 mV	5.3 mV

Notes:
6. Wideband noise aliased into the baseband. Referred to the input. Typical values shown for 25 °C.
7. For Peak-to-Peak Noise multiply by 6.6 for all ranges and output rates.
8. For input ranges <100 mV and output word rates >60 Hz, 32.768 kHz chopping frequency is used.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter			Min	Typ	Max	Unit
Analog Input						
Common Mode + Signal on AIN+ or AIN-		Bipolar/Unipolar Mode				
NBV = -1.8 to -2.5 V	Range = 25 mV, 55 mV, or 100 mV		-0.150	-	0.950	V
	Range = 1 V, 2.5 V, or 5 V		NBV	-	VA+	V
NBV = AGND	Range = 25 mV, 55 mV, or 100 mV		1.85	-	2.65	V
	Range = 1 V, 2.5 V, or 5 V		0.0	-	VA+	V
Common Mode Rejection	dc		-	120	-	dB
	50, 60 Hz		-	120	-	dB
Input Capacitance			-	10	-	pF
CVF Current on AIN+ or AIN-		(Note 5)				
	Range = 25 mV, 55 mV, or 100 mV		-	100	300	pA
	Range = 1 V, 2.5 V, or 5 V		-	1.2	-	µA/V
System Calibration Specifications						
Full Scale Calibration Range		Bipolar/Unipolar Mode (Note 9)				
	25 mV		17.5	-	32.5	mV
	55 mV		38.5	-	71.5	mV
	100 mV		70	-	105	mV
	1 V		0.70	-	1.30	V
	2.5 V		1.75	-	3.25	V
	5 V		3.50	-	VA+	V
Offset Calibration Range		Bipolar/Unipolar Mode				
	25 mV		-	-	±12.5	mV
	55 mV		-	-	±27.5	mV
	100 mV	(Note 10)	-	-	±50	mV
	1 V		-	-	±0.5	V
	2.5 V		-	-	±1.25	V
	5 V		-	-	±2.50	V
Power Supplies						
DC Power Supply Currents (Normal Mode)		I_{A+}	-	1.65	2.2	mA
		I_{D+}	-	15	30	µA
		I_{NBV}	-	475	700	µA
Power Consumption	Normal Mode	(Note 11)	-	9.4	12.7	mW
	Low Power Mode		-	4.9	8.5	mW
	Standby		-	1.2	-	mW
	Sleep		-	500	-	µW
Power Supply Rejection	dc Positive Supplies		-	95	-	dB
	dc NBV		-	110	-	dB

Notes: 9. The minimum Full Scale Calibration Range (FSCR) is limited by the maximum allowed gain register value (with margin). The maximum FSCR is limited by the ΔΣ modulator's 1's density range.

10. The maximum full scale signal can be limited by saturation of circuitry within the internal signal path.

11. All outputs unloaded. All input CMOS levels.

5 V DIGITAL CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5 V ±5%; GND = 0; See Notes 2 and 12.))

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	All Pins Except XIN and SCLK	V_{IH}	0.6 VD+	-	-	V
	XIN		3.5	-	VD+	V
	SCLK		(VD+) - 0.45	-	-	V
Low-Level Input Voltage	All Pins Except XIN and SCLK	V_{IL}	-	-	0.8	V
	XIN		0.0	-	1.5	V
	SCLK		-	-	0.6	V
High-Level Output Voltage		V_{OH}				
	All Pins Except CPD and SDO (Note 13)		(VA+) - 1.0	-	-	V
	CPD, I_{out} = -4.0 mA		(VD+) - 1.0	-	-	V
	SDO, I_{out} = -5.0 mA		(VD+) - 1.0	-	-	V
Low-Level Output Voltage		V_{OL}				
	All Pins Except CPD and SDO, I_{out} = 1.6 mA		-	-	0.4	V
	CPD, I_{out} = 2 mA		-	-	0.4	V
	SDO, I_{out} = 5.0 mA		-	-	0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Notes: 12. All measurements performed under static conditions.

13. I_{out} = -100 µA unless stated otherwise. (V_{OH} = 2.4 V @ I_{out} = -40 µA.)

3.0 V DIGITAL CHARACTERISTICS (T_A = 25 °C; VA+ = 5 V ±5%; VD+ = 3.0 V ±10%; GND = 0; See Notes 2 and 12.))

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	All Pins Except XIN and SCLK	V_{IH}	0.6 VD+	-	-	V
	XIN		0.54 VA+	-	VD+	V
	SCLK		(VD+) - 0.45	-	-	V
Low-Level Input Voltage	All Pins Except XIN and SCLK	V_{IL}	-	-	0.16 VD+	V
	XIN		0.0	-	1.5	V
	SCLK		-	-	0.6	V
High-Level Output Voltage		V_{OH}				
	All Pins Except CPD and SDO, I_{out} = -400 µA		(VA+) - 0.3	-	-	V
	CPD, I_{out} = -4.0 mA		(VD+) - 1.0	-	-	V
	SDO, I_{out} = -5.0 mA		(VD+) - 1.0	-	-	V
Low-Level Output Voltage		V_{OL}				
	All Pins Except CPD and SDO, I_{out} = 400 µA		-	-	0.3	V
	CPD, I_{out} = 2 mA		-	-	0.4	V
	SDO, I_{out} = 5.0 mA		-	-	0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Unit
Modulator Sampling Frequency	f_s	XIN/2	Hz
Filter Settling Time to 1/2 LSB (Full Scale Step)	t_s	$1/f_{out}$	s

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0 V; See Note 14.))

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	Positive Digital	VD+	2.7	5.0	5.25	V
	Positive Analog	VA+	4.75	5.0	5.25	V
Analog Reference Voltage	(VREF+) - (VREF-)	$VRef_{diff}$	1.0	2.5	3.0	V
Negative Bias Voltage		NBV	-1.8	-2.1	-2.5	V

Notes: 14. All voltages with respect to ground.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V; See Note 14.)

Parameter		Symbol	Min	Max	Unit
DC Power Supplies	(Note 15)				
	Positive Digital	VD+	-0.3	+6.0	V
	Positive Analog	VA+	-0.3	+6.0	V
Negative Bias Voltage	Negative Potential	NBV	+0.3	-3.0	V
Input Current, Any Pin Except Supplies	(Note 16 and 17)	I_{IN}	-	±10	mA
Output Current		I_{OUT}	-	±25	mA
Power Dissipation	(Note 18)	PDN	-	500	mW
Analog Input Voltage	VREF pins	V_{INR}	-0.3	(VA+) + 0.3	V
	AIN Pins	V_{INA}	NBV - 0.3	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 15. No pin should go more negative than NBV - 0.3 V.

16. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pins.

17. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

18. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = 25 °C; VA+ = 5 V ±5%; VD+ = 3.0 V ±10% or 5 V ±5%; Input Levels: Logic 0 = 0 V, Logic 1 = VD+; C_L = 50 pF.))

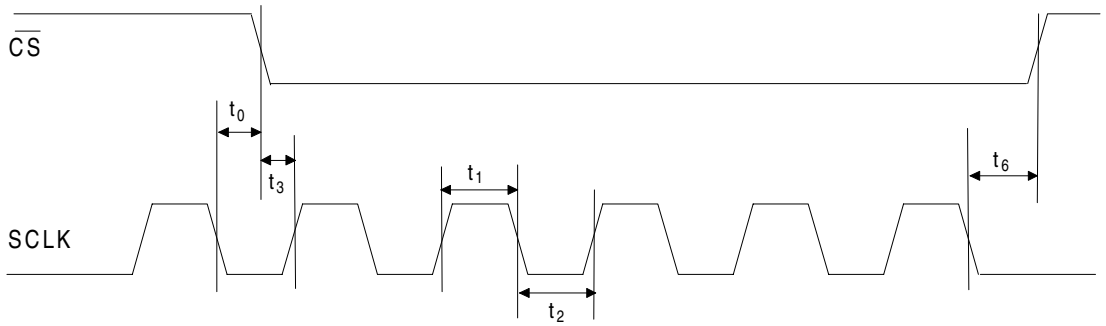
Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency (Note 19)	XIN				
Internal Clock		30	32.768	36	kHz
External Clock		30	32.768	100	
Master Clock Duty Cycle		40	-	60	%
Rise Times (Note 20)	t_{rise}				
Any Digital Input Except SCLK		-	-	1.0	µs
SCLK		-	-	100	µs
Any Digital Output		-	50	-	ns
Fall Times (Note 20)	t_{fall}				
Any Digital Input Except SCLK		-	-	1.0	µs
SCLK		-	-	100	µs
Any Digital Output		-	50	-	ns
Start-up					
Oscillator Start-up Time XTAL = 32.768 kHz (Note 21)	t_{ost}	-	500	-	ms
Power-on Reset Period	t_{por}	-	1003	-	XIN cycles
Serial Port Timing					
Serial Clock Frequency	SCLK	0	-	2	MHz
SCLK Falling to $\overline{CS}$ Falling for continuous running SCLK (Note 22)	t_0	100	-	-	ns
Serial Clock Pulse Width High	t_1	250	-	-	ns
Pulse Width Low	t_2	250	-	-	ns
SDI Write Timing					
$\overline{CS}$ Enable to Valid Latch Clock	t_3	50	-	-	ns
Data Set-up Time prior to SCLK rising	t_4	50	-	-	ns
Data Hold Time After SCLK Rising	t_5	100	-	-	ns
SCLK Falling Prior to $\overline{CS}$ Disable	t_6	100	-	-	ns
SDO Read Timing					
$\overline{CS}$ to Data Valid	t_7	-	-	150	ns
SCLK Falling to New Data Bit	t_8	-	-	150	ns
$\overline{CS}$ Rising to SDO Hi-Z	t_9	-	-	150	ns

Notes: 19. Device parameters are specified with a 32.768 kHz clock; however, clocks up to 100 kHz can be used for increased throughput.

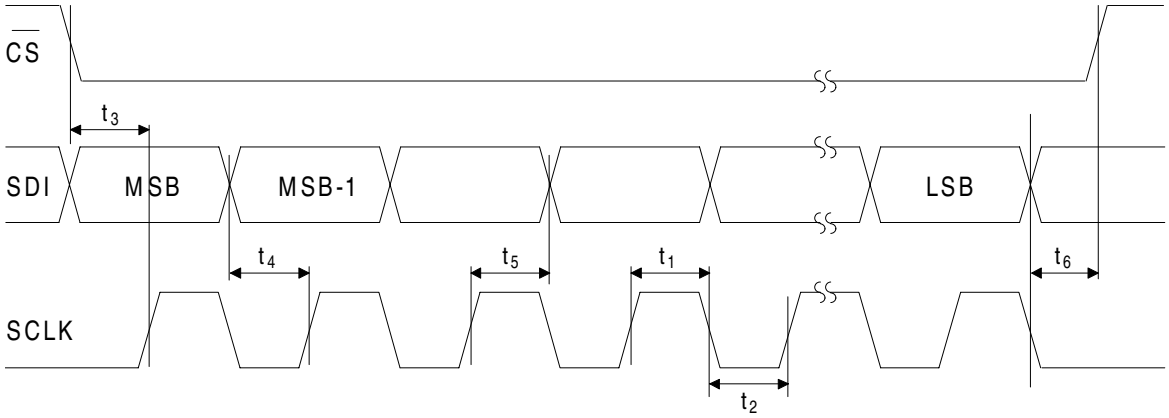
20. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

21. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

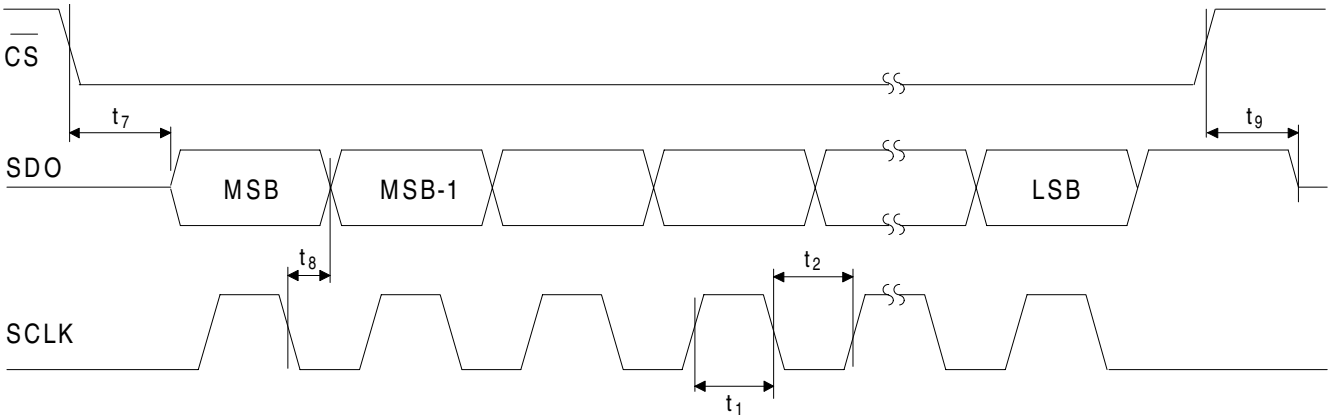
22. Applicable when SCLK is continuously running.



Continuous Running SCLK Timing (Not to Scale)



SDI Write Timing (Not to Scale)



SDO Read Timing (Not to Scale)

DETAILED DESCRIPTION

The CS5525 and CS5526 are 16-bit and 20-bit pin compatible converters which include a chopper-stabilized instrumentation amplifier input, and an on-chip programmable gain amplifier. They are both optimized for measuring low-level unipolar or bipolar signals in process control and medical applications.

The CS5525/26 also include a fourth order delta-sigma modulator, a calibration microcontroller, eight digital filters, a 4-bit analog latch, and a serial port. The digital filters provide any one of eight different output update rates.

The CS5525/26 include a CPD (Charge Pump Drive) output (shown in Figure 1). CPD provides a negative bias voltage to the on-chip instrumentation amplifier when used with a combination of external diodes and capacitors. This enables the CS5525/26 to measure negative voltages with respect to ground, making the converters ideal for thermocouple temperature measurements.

Theory of Operation

The CS5525/26 A/D converters are designed to operate from a single +5 V analog supply and provide several different input ranges. See the ***Analog Characteristics*** section on page 3 for details.

Figure 1 illustrates the CS5525/26 connected to generate their own negative bias supply using the on-chip CPD (Charge Pump Drive). This enables the CS5525/26 to measure ground referenced signals with magnitudes down to NBV (Negative Bias Voltage, approximately -2.1 V in this example). Figure 2 illustrates a charge pump circuit when the converters are powered from a +3.0 V digital supply. Alternatively, the negative bias supply can be generated from a negative supply voltage or a resistive divider as illustrated in Figure 3.

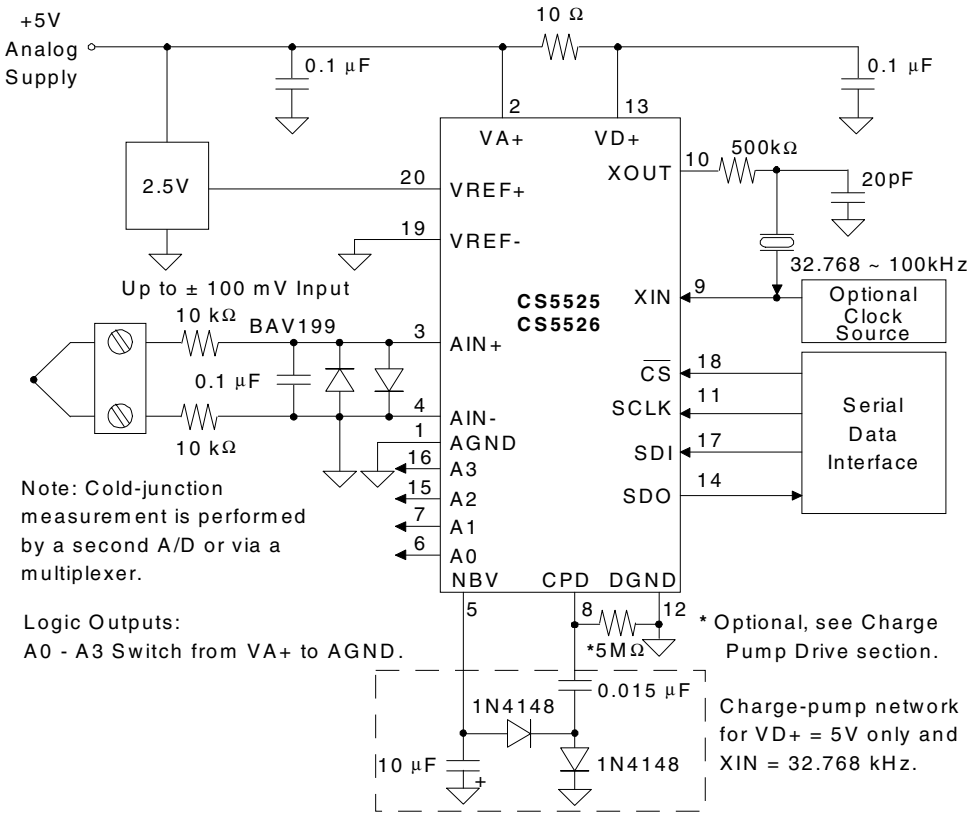


Figure 1. CS5525/26 Configured to use on-chip charge pump to supply NBV.

Figure 4 illustrates the CS5525/26 connected to measure ground referenced unipolar signals of a positive polarity using the 1 V, 2.5 V, and 5 V input voltage ranges on the converter. For the 25 mV, 55 mV, and 100 mV ranges the signal must have a common mode near +2.5 V (NBV = 0V).

The CS5525/26 are optimized for the measurement of thermocouple outputs, but they are also well suited for the measurement of ratiometric bridge transducer outputs. Figure 5 illustrates the CS5525/26 connected to measure the output of a ratiometric differential bridge transducer while operating from a single +5 V supply.

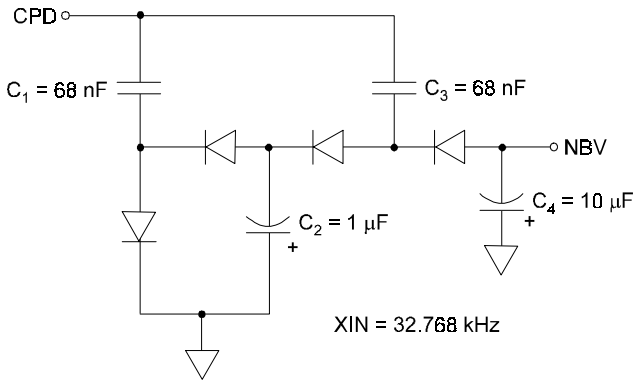


Figure 2. Charge Pump Drive Circuit for VD+ = 3 V.

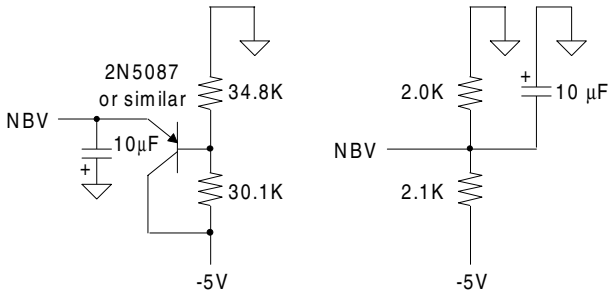


Figure 3. Alternate NBV Circuits.

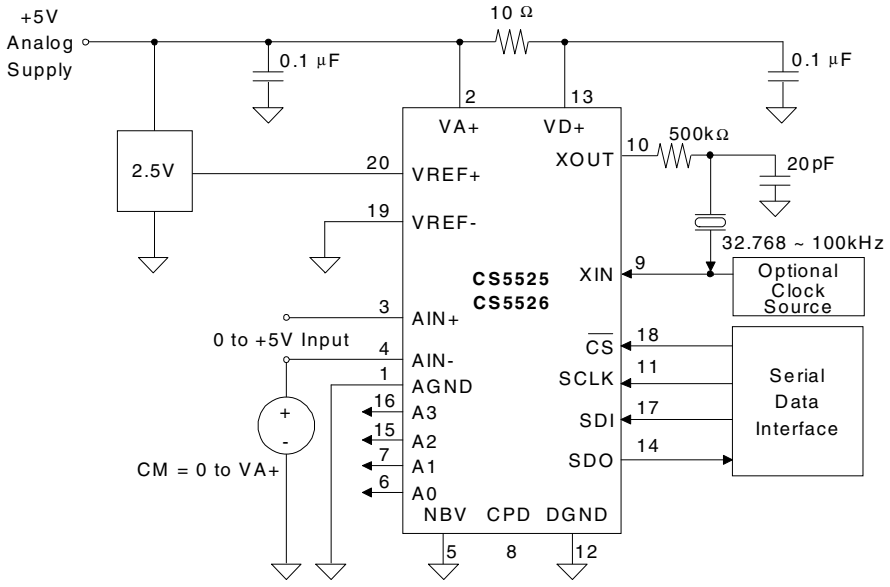


Figure 4. CS5525/26 Configured for ground-referenced Unipolar Signals.

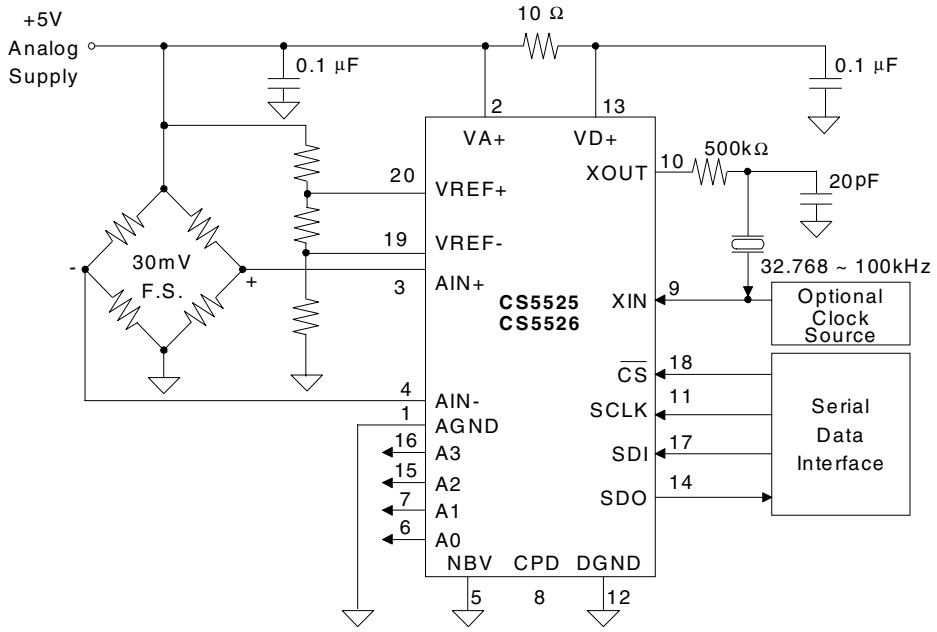


Figure 5. CS5525/26 Configured for Single Supply Bridge Measurement.

System Initialization

When power to the CS5525/26 is applied, they are held in a reset condition until their 32.768 kHz oscillators have started and their start-up counter-timer elapses. Due to the high Q of a 32.768 kHz crystal, the oscillators take 400-600 ms to start. The converter's counter-timer counts no more than 1024 oscillator clock cycles to make sure the oscillator is fully stable. During this time-out period the serial port logic is reset and the RV (Reset Valid) bit in the configuration register is set. A reset can be initiated at any time by writing a logic 1 to the RS (Reset System) bit in the configuration register. This automatically sets the RV bit until the RS bit is written to logic 0, and the configuration register is read. After a reset, the on-chip registers are initialized to the following states and the converters are ready to perform conversions.

configuration register:	000040(H)
offset register:	000000(H)
gain register:	800000(H)

Command Operation

The CS5525/26 include a microcontroller with five registers used to control the converter. Each register is 24-bits in length except the 8-bit command register (command, configuration, offset, gain, and conversion data). After a system initialization or reset, the serial port is initialized to the command mode and the converter stays in this mode until a valid 8-bit command is received (the first 8-bits into the serial port). Table 1 lists all the valid commands. Once a valid 8-bit command (a read or a write command word) is received and interpreted by the command register, the serial port enters the data mode. In data mode the next 24 serial clock pulses shift data either into or out of the serial port (72 serial clock pulses are needed if set-up register is selected). See Table 2 for configuring the CS5525/26.

Reading/Writing On-Chip Registers

The CS5525/26's offset, gain, and configuration registers are read/writable while the conversion data register is read only.

To perform a read from a specific register, the R/$\overline{W}$ bit of the command word must be a logic 1. The SC, CC, and PS/$\overline{R}$ bits must be logic 0 and the CB (MSB) bit must be a logic 1. The register to be written is selected with the RSB2-RSB0 bits of the command word.

To perform a write to a specific register, the R/$\overline{W}$ bit of the command word must be a logic 0. The SC, CC, and PS/R bits must be logic 0 and the CB (MSB) bit must be a logic 1. The register to be written is selected with the RSB2-RSB0 bits of the command word. Figure 6 illustrates the serial sequence necessary to write to, or read from the serial port.

If the Set-up Registers are chosen with the RSB2-RSB0 bits, the registers are read or written in the following sequence: Offset, Gain and Configuration. This is accomplished by following one 8-bit command word with three 24-bit data words for a total of 72 data bits.

Command Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
CB	SC	CC	R/$\overline{W}$	RSB2	RSB1	RSB0	PS/$\overline{R}$

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, CB	0 1	Null command (no operation). All command bits, including CB must be 0. Logic 1 for executable commands.
D6	Single Conversion, SC	0 1	Single Conversion not active. Perform a conversion.
D5	Continuous Conversions, CC	0 1	Continuous Conversions not active. Perform conversions continuously.
D4	Read/Write, R/$\overline{W}$	0 1	Write to selected register. Read from selected register.
D3-D1	Register Select Bit, RSB2-RSB0	000 001 010 011 100 101 110 111	Offset Register Gain Register Configuration Register Conversion Data Register (read only) Set-up Registers (Offset, Gain, Configuration) Reserved Reserved Reserved
D0	Power Save/$\overline{Run}$, PS/$\overline{R}$	0 1	Run Power Save

Table 1. Command Set

Configuration Register

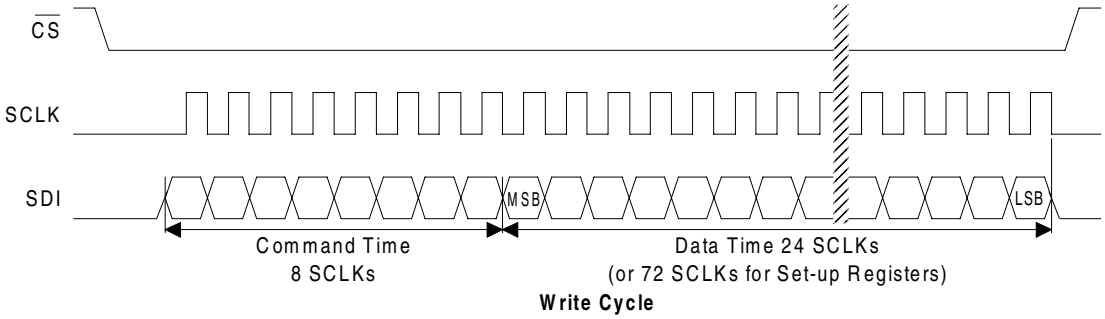
D23(MSB)	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
A3	A2	A1	A0	NU	CFS	NU	LPM	WR2	WR1	WR0	U/$\overline{B}$

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
G2	G1	G0	PD	RS	RV	PF	PSS	DF	CC2	CC1	CC0

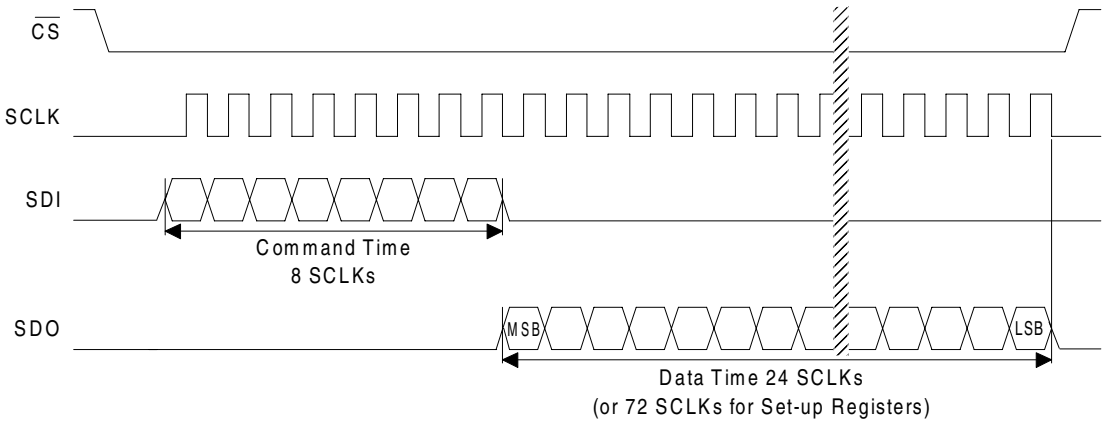
BIT	NAME	VALUE		FUNCTION
D23-D20	Latch Outputs, A3-A0	0000	R*	Latch Output Pins A3-A0 mimic the D23-D20 Register bits.
D19	Not Used, NU	0	R	Must always be logic 0.
D18	Chop Frequency Select, CFS	0 1	R	256 Hz Amplifier chop frequency 32768 Hz Amplifier chop frequency
D17	Not Used, NU	0	R	Must always be logic 0.
D16	Low Power Mode, LPM	0 1	R	Normal Mode Reduced Power mode
D15-D13	Word Rate, WR2-0 Note: For XIN = 32.768kHz	000 001 010 011 100 101 110 111	R	15.0 Hz (2182 XIN cycles) 30.1 Hz (1090 XIN cycles) 60.0 Hz (546 XIN cycles) 123.2 Hz (266 XIN cycles) 168.9 Hz (194 XIN cycles) 202.3 Hz (162 XIN cycles) 3.76 Hz (8722 XIN cycles) 7.51 Hz (4362 XIN cycles)
D12	Unipolar/$\overline{\text{Bipolar}}$, U/$\overline{B}$	0 1	R	Bipolar Measurement mode Unipolar Measurement mode
D11-D9	Gain Bits, G2-G0	000 001 010 011 100 101 110/111	R	100 mV (assumes VREF = 2.5V) 55 mV 25 mV 1 V 5.0 V 2.5 V Not Used.
D8	Pump Disable, PD	0 1	R	Charge Pump Enabled For PD = 1, the CPD pin goes to a Hi-Z output state.
D7	Reset System, RS	0 1	R	Normal Operation Activate a Reset cycle. To return to Normal Operation write bit to zero.
D6	Reset Valid , RV	0 1	 R	No reset has occurred or bit has been cleared (read only). Valid Reset has occurred. (Cleared when read.)
D5	Port Flag, PF	0 1	R	Port Flag mode inactive Port Flag mode active
D4	Power Save Select, PSS	0 1	R	Standby Mode (Oscillator active, allows quick power-up) Sleep Mode (Oscillator inactive)
D3	Done Flag, DF	0 1	R	Done Flag bit is cleared (read only). Calibration or Conversion cycle completed (read only).
D2-D0	Calibration Control Bits, CC2-CC0	000 001 010 011 100 101 110 111	R	Normal Operation (no calibration) Offset -- Self-Calibration Gain -- Self-Calibration Offset Self-Calibration followed by Gain Self-Calibration Not used. Offset -- System Calibration Gain -- System Calibration Not Used.

* R indicates the bit value after the part is reset

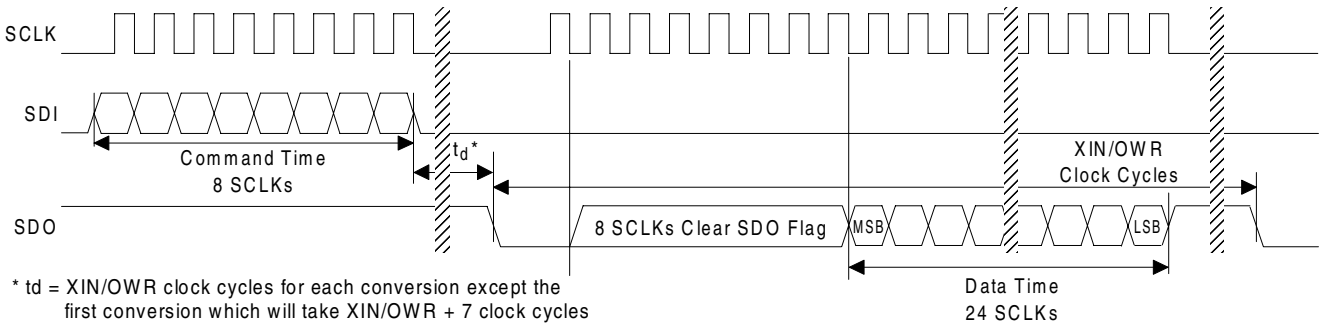
Table 2. Configuration Register



Write Cycle



Read Cycle



SDO Continuous Conversion Read (PF bit = 1)

Figure 6. Command and Data Word Timing.

Analog Input

Figure 7 illustrates a block diagram of the analog input signal path inside the CS5525/26. The front end consists of a chopper-stabilized instrumentation amplifier with 20X gain and a programmable gain section. The instrumentation amplifier is powered from VA+ and from the NBV (Negative Bias Voltage) pin allowing the CS5525/26 to be operated in either of two analog input configurations. The NBV pin can be biased to a negative voltage between -1.8 V and -2.5 V, or tied to AGND. The choice of the operating mode for the NBV voltage depends upon the input signal and its common mode voltage.

For the 25 mV, 55 mV, and 100 mV input ranges, the input signals to AIN+ and AIN- are amplified by the 20X instrumentation amplifier. For ground referenced signals with magnitudes less then 100 mV, the NBV pin should be biased with -1.8 V to -2.5 V. If NBV is tied between -1.8 V and -2.5 V, the (Common Mode + Signal) input on AIN+ and AIN- must stay between -0.150 V and 0.950 V to ensure proper operation. Alternatively, NBV can be tied to AGND where the input (Common Mode + Signal) on AIN+ and AIN- must stay between 1.85 V and 2.65 V to ensure that the amplifier operates properly.

For the 1 V, 2.5 V, and 5 V input ranges, the instrumentation amplifier is bypassed and the input signals are directly connected to the Programmable Gain block. With NBV tied between -1.8 V and -2.5 V, the (Common Mode + Signal) input on AIN+ and AIN- must stay between NBV and VA+. Alternatively, NBV can be tied to AGND where the input (Common Mode + Signal) on AIN+ and AIN- pins can span the entire range between AGND and VA+.

The CS5525/26 can accommodate full scale ranges other than 25 mV, 55 mV, 100 mV, 1 V, 2.5 V and 5 V by performing a system calibration within the limits specified. See the **Calibration** section for more details. Another way to change the full scale range is to increase or to decrease the voltage reference to other than 2.5 V. See the **Voltage Reference** section for more details.

Three factors set the operating limits for the input span. They include: instrumentation amplifier saturation, modulator 1's density, and a lower reference voltage. When the 25 mV, 55 mV or 100 mV range is selected, the input signal (including the common mode voltage and the amplifier offset voltage) must not cause the 20X amplifier to saturate in either its input stage or output stage. To prevent saturation the absolute voltages on AIN+ and AIN- must stay within the limits specified (refer to the '***Analog Input***' table on page 3). Additionally, the differential output voltage of the amplifier must not exceed 2.8 V. The equation

$$ABS(VIN + VOS) \times 20 = 2.8\ V$$

defines the differential output limit, where

$$VIN = (AIN+) - (AIN-)$$

is the differential input voltage and VOS is the absolute maximum offset voltage for the instrumentation amplifier (VOS will not exceed 40 mV). If the

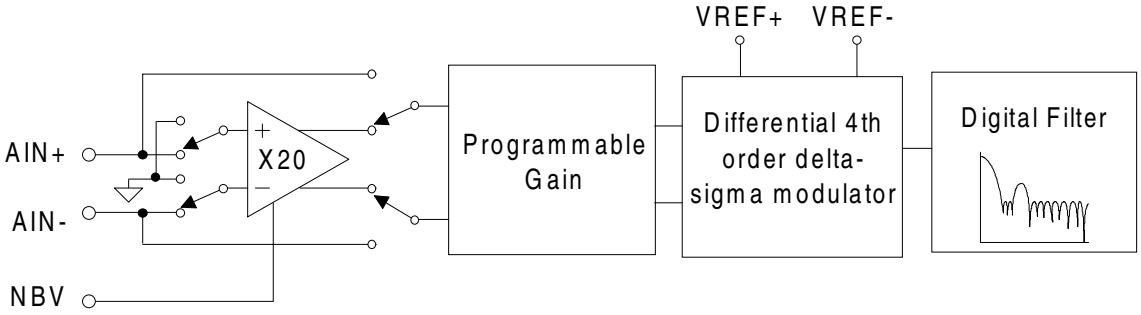


Figure 7. Block Diagram of Analog Signal Path

Input Range(1)	Max. Differential Output 20X Amplifier	VREF	Gain Factor	Δ-Σ Nominal(1) Differential Input	Δ-Σ(1) Max. Input
± 25 mV	2.8 V (2)	2.5V	5	± 0.5 V	± 0.75 V
± 55 mV	2.8 V (2)	2.5V	2.272727...	± 1.1 V	± 1.65 V
± 100 mV	2.8 V (2)	2.5V	1.25	± 2.0 V	± 3.0 V
± 1.0 V	-	2.5V	2.5	± 1.0 V	± 1.5 V
± 2.5 V	-	2.5V	1.0	± 2.5 V	± 5.0 V
± 5.0 V	-	2.5V	0.5	± 5.0 V	0V, VA+

Note: 1. The converter's actual input range, the delta-sigma's nominal full scale input, and the delta-sigma's maximum full scale input all scale directly with the value of the voltage reference. The values in the table assume a 2.5 V VREF voltage.

Table 3. Relationship between Full Scale Input, Gain Factors, and Internal Analog Signal Limitations

differential output voltage from the amplifier exceeds 2.8 V, the amplifier may saturate, which will cause a measurement error.

The input voltage into the modulator must not cause the modulator to exceed a low of 20 percent or a high of 80 percent 1's density. The nominal full scale input span of the modulator (from 30 percent to 70 percent 1's density) is determined by the VREF voltage divided by the Gain Factor. See Table 3 to determine if the CS5525/26 are being used properly. For example, in the 55 mV range to determine the nominal input voltage to the modulator, divide VREF (2.5 V) by the Gain Factor (2.2727).

When a smaller voltage reference is used, the resulting code widths are smaller causing the converter output codes to exhibit more changing codes for a fixed amount of noise. Table 3 is based upon a VREF = 2.5 V. For other values of VREF, the values in Table 3 must be scaled accordingly.

Figure's 8 and 9 illustrate the input models for the AIN and VREF pins. The dynamic input current for each of the pins can be determined from the models shown and is dependent upon the setting of the CFS (Chop Frequency Select) bit. The effective input impedance for the AIN+ and AIN- pins remains constant for the three low level measurement ranges (25 mV, 55 mV, and 100 mV). The input current is lowest with the CFS bit cleared to logic 0.

Note: *Residual noise appears in the converter's baseband for output word rates greater than 60 Hz if CFS is logic 0. By setting CFS to logic 1, the amplifier's chop frequency chops at 32768 Hz eliminating the residual noise, but increasing the current. Note that C=48pF is for input current modeling only. For physical input capacitance see 'Input Capacitance' specification under 'Analog Characteristics' on page 3.*

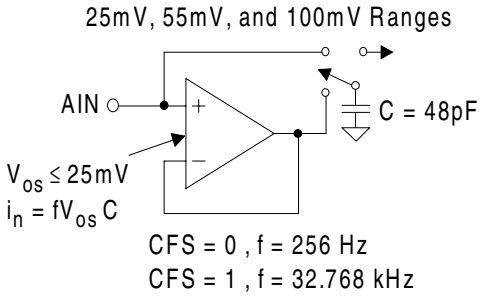


Figure 8. Input models for AIN+ and AIN- pins

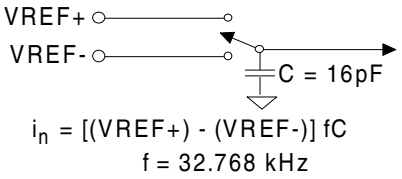


Figure 9. Input model for VREF+ and VREF- pins.

Charge Pump Drive

The CPD (Charge Pump Drive) pin of the converters can be used with external components (shown in Figure 1) to develop an appropriate negative bias voltage for the NBV pin. When CPD is used to generate the NBV, the NBV voltage is regulated with an internal regulator loop referenced to VA+. Therefore, any change on VA+ results in a proportional change on NBV. With VA+ = 5 V, NBV's regulation is set proportional to VA+ at approximately -2.1 V.

Figure 3 illustrates a means of supplying NBV voltage from a -5 V supply. For ground based signals with the instrumentation amplifier engaged (when in the 25mV, 55mV, or 100mV ranges), the voltage on the NBV pin should at no time be less negative than -1.8 V or more negative than -2.5 V. To prevent excessive voltage stress to the chip the NBV voltage should not be more negative than -3.0 V.

The components in Figure 1 are the preferred components for the CPD filter. However, smaller capacitors can be used with acceptable results. The 10 μF ensures very low ripple on NBV. Intrinsic safety requirements prohibit the use of electrolytic capacitors. In this case, two 0.47 μF ceramic capacitors in parallel can be used.

The CPD pin itself is a tri-state output and enters tri-state whenever the converters are placed into the Sleep Mode, Standby Mode, or when the charge pump is disabled (when the Pump Disable bit, bit D8 in the configuration register, is set). Once in tri-state, the digital current can increase if this CPD output floats near 1/2 digital supply. To ensure the CPD pin stays near ground and to minimize the digital current, add a 5MΩ resistor between it and DGND (see Figure 1). If the resistor is left out, the digital supply current may increase from 2 μA to 10 μA.

Voltage Reference

The CS5525/26 are specified for operation with a 2.5 V reference voltage between the VREF+ and VREF- pins of the devices. For a single-ended reference voltage, such as the LT1019-2.5, the reference's output is connected to the VREF+ pin of the CS5525/26. The ground reference for the LT1019-2.5 is connected to the VREF- pin.

The differential voltage between the VREF+ and VREF- can be any voltage from 1.0 V up to 3.0 V, however, the VREF- pin can not go below analog ground.

Calibration

The CS5525/26 offer five different calibration functions including self calibration and system calibration. However, after the CS5525/26 are reset, they can perform measurements without being calibrated. In this case, the converters will utilize the initialized values of the on-chip registers (Gain = 1.0, Offset = 0.0) to calculate output words for the ±100 mV range. Any initial offset and gain errors in the internal circuitry of the chips will remain.

The gain and offset registers, which are used for both self and system calibration, are used to set the zero and full-scale points of the converter's transfer function. One LSB in the offset register is 2^{-24} proportion of the input span (bipolar span is 2 times the unipolar span). The MSB in the offset register determines if the offset to be trimmed is positive or negative (0 positive, 1 negative). The converters can typically trim ±50 percent of the input span. The gain register spans from 0 to $(2 - 2^{-23})$. The decimal equivalent meaning of the gain register is

$$D = b_0 2^0 + b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N} = \sum_{i=0}^{N} b_i 2^{-i}$$

where the binary numbers have a value of either zero or one (b_0 corresponds to the MSB). Refer to Table 4 for details.

Offset Register

	MSB											LSB
Register	Sign	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}
Reset (R)	0	0	0	0	0	0	0	0	0	0	0	0

One LSB represents 2^{-24} proportion of the input span (bipolar span is 2 times unipolar span)
Offset and data word bits align by MSB (bit MSB-4 of offset register changes bit MSB-4 of data)

Gain Register

	MSB											LSB
Register	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}
Reset (R)	1	0	0	0	0	0	0	0	0	0	0	0

The gain register span is from 0 to ($2-2^{-23}$). After Reset the MSB = 1, all other bits are 0.

Table 4. Offset and Gain Registers

The offset and gain calibration steps each take one conversion cycle to complete. At the end of the calibration step, the calibration control bits will be set back to logic 0, and the DF (Done Flag) bit will be set to a logic 1. For the combination self-calibration (CC2-CC0= 011; offset followed by gain), the calibration will take two conversion cycles to complete and will set the DF bit after the gain calibration is completed. The DF bit will be cleared any time the data register, the offset register, the gain register, or the setup register is read. Reading the configuration register alone will not clear the DF bit.

Self Calibration

The CS5525/26 offer both self offset and self gain calibrations. For the self-calibration of offset in the 25 mV, 55 mV, and 100 mv ranges, the converter internally ties the inputs of the instrumentation amplifier together and routes them to the AIN- pin as shown in Figure 10. For proper self-calibration of offset to occur in the 25 mV, 55 mV, and 100 mV ranges, the AIN- pin must be at the proper common-mode-voltage (i.e. AIN- = 0V, NBV must be between -1.8 V to -2.5 V). For self-calibration of offset in the 1.0 V, 2.5 V, and 5 V ranges, the inputs of the modulator are connected together and then routed to the VREF- pin as shown in Figure 11.

For self-calibration of gain, the differential inputs of the modulator are connected to VREF+ and

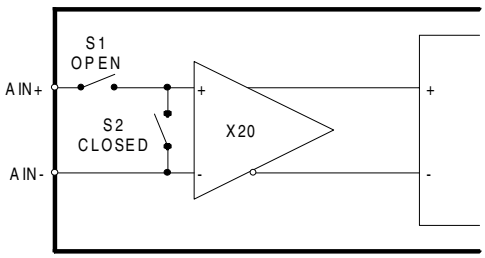


Figure 10. Self Calibration of Offset (Low Ranges).

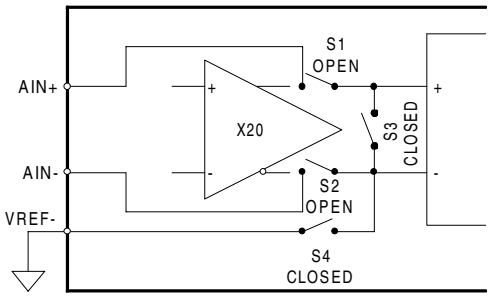


Figure 11. Self Calibration of Offset (High Ranges).

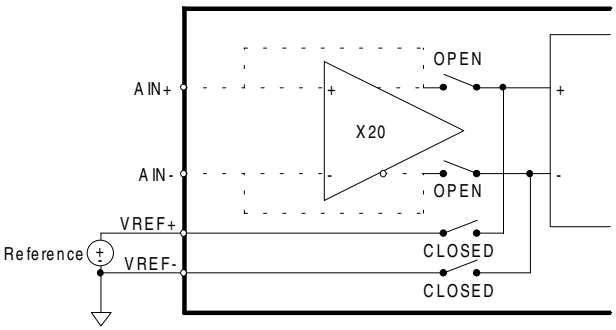


Figure 12. Self Calibration of Gain (All Ranges).

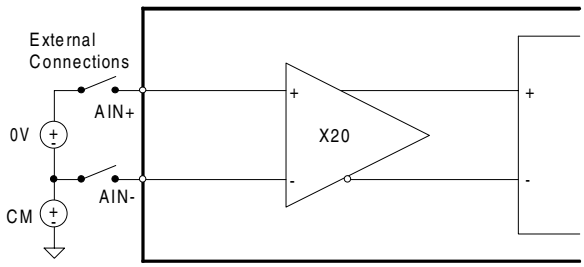


Figure 13. System Calibration of Offset (Low Ranges).

VREF- as shown in Figure 12. For any input range other than the 2.5 V range, the modulator gain error can not be completely calibrated out. This is due to the lack of an accurate full scale voltage internal to the chips. The 2.5 V range is an exception because the external reference voltage is 2.5 V nominal and is used as the full scale voltage. In addition, when self-calibration of gain is performed in the 25 mV, 55 mV, and 100 mV input ranges, the instrumentation amplifier's gain is not calibrated. These two factors can leave the converters with a gain error of up to ±20% after self-calibration of gain. Therefore, a system gain is required to get better accuracy, except for the 2.5 V range.

System Calibration

For the system calibration functions, the user must supply the converters calibration signals which represent ground and full scale. When a system offset calibration is performed, a ground reference signal must be applied to the converter. See Figures 13 and 14. As shown in Figures 15 and 16, the user must input a signal representing the positive full scale point to perform a system gain calibration. In either case, the calibration signals must be within the specified calibration limits for each specific calibration step (refer to the System Calibration Specifications).

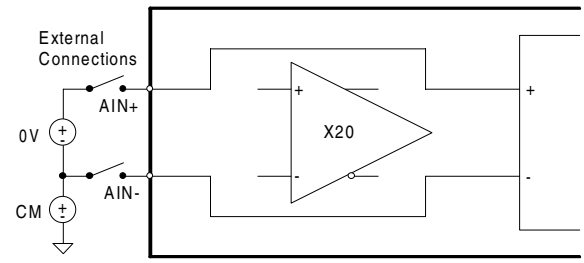


Figure 14. System Calibration of Offset (High Ranges).

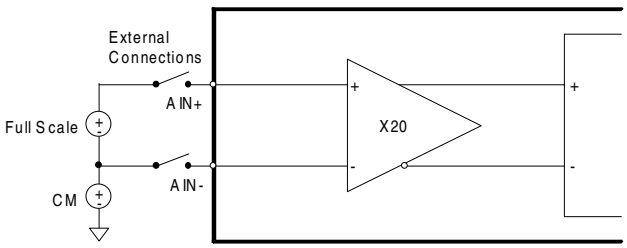


Figure 15. System Calibration of Gain (Low Ranges)

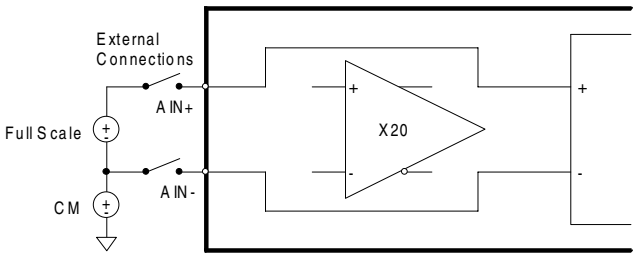


Figure 16. System Calibration of Gain (High Ranges).

Assuming a system can provide two known voltages, equations can allow the user to manually compute the calibration register's values based on two uncalibrated conversions. The offset and gain calibration registers are used to adjust a typical conversion as follows:

$$Rc = (Ru + Co>>4) * Cg / 2^{23}.$$

Calibration can be performed using the following equations:

$$Co = (Rc0/G - Ru0) << 4$$

$$Cg = 2^{23} * G$$

$$\text{where } G = (Rc1 - Rc0)/(Ru1-Ru0).$$

Note: *Uncalibrated conversions imply that the gain and offset registers are at default {gain register = 0x800000 (Hex) and offset register = 0x000000 (Hex)}.*

The variables are defined below.

V0	=	First calibration voltage
V1	=	Second calibration voltage (greater than V0)
Ru	=	Result of any uncalibrated conversion
Ru0	=	Result of uncalibrated conversion V0 (20-bit integer or 2's complement)
Ru1	=	Result of uncalibrated conversion of V1 (20-bit integer or 2's complement)
Rc	=	Result of any conversion
Rc0	=	Desired calibration result of converting V0 (20-bit integer or 2's complement)
Rc1	=	Desired calibration result of converting V1 (20-bit integer or 2's complement)
Co	=	Offset calibration register value (24-bit 2's complement)
Cg	=	Gain calibration register value (24-bit integer)
>>	=	The shift right operator (e.g. x >>2 is x shifted right 2 bits)
<<	=	The shift left operator (e.g. x<<2 is x shifted left 2 bits)

Note: *The shift operators are used here to align the decimal points of words of various lengths. Data to the right of the decimal point may be used in the calculations shown. For the CS5525 all conversion results (Ru, Rc...) are 16 bits instead of 20 bits. To get the equations to work correctly pad the 16 bit results with four zeros (on the right).*

Calibration Tips

Calibration steps are performed at the output word rate selected by the WR2-WR0 bits of the configuration register. Since higher word rates result in conversion words with more peak-to-peak noise, calibration should be performed at lower output word rates. Also, to minimize digital noise near the devices, the user should wait for each calibration step to be completed before reading or writing to the serial port.

For maximum accuracy, calibrations should be performed for offset and gain for each gain setting (selected by changing the G2-G0 bits of the configuration register). And if factory calibration is performed using the system calibration capabilities of the CS5525/26, the offset and gain register contents can be read by the system microcontroller and recorded in EEPROM. These same calibration words can then be uploaded into the offset and gain registers of the converters when power is first applied to the system, or when the gain range is changed.

Two final tips include two ways to determine when calibration is complete: 1) wait for SDO to fall. It falls to logic 0 if the PF (Port Flag) bit of the configuration register is set to logic 1; or 2) poll the DF (Done Flag) bit in the configuration register which is set at completion of calibration. Whichever method is used, the calibration control bits (CC2-CC0) will return to logic 0 upon completion of any calibration.

Limitations in Calibration Range

System calibration can be limited by signal headroom in the analog signal path inside the chip as discussed under the ***Analog Input*** section of this data sheet. System calibration can also be limited by the intrinsic gain errors of the instrumentation amplifier and the modulator. For gain calibrations

the input signal can be reduced to the point in which the gain register reaches its upper limit of 2.0 (decimal) [FFFFFF Hex] (this is most likely to occur with an input signal approximately 1/2 the nominal range). Alternatively, the input signal can be increased to a point in which the modulator reaches its one's density upper limit of 80% (this is most likely to occur with an input signal approximately 1.5 times the nominal range). Also, for full scale inputs larger than the nominal full scale value of the range selected, there is some voltage at which the various internal circuits may saturate due to limited amplifier headroom (this is most likely to occur on the 100 mV range setting when NBV = -1.8 V).

Analog Output Latch Pins

The A3-A0 pins of the converters mimic the D23-D20 bits of the configuration register. A3-A0 can be used to control multiplexers and other logic functions outside the converter. The outputs can sink or source at least 1 mA, but it is recommended to limit drive currents to less than 2 µA to reduce self-heating of the chip. These outputs are powered from VA+, hence, their output voltage for a logic 1 will be limited to the VA+ voltage.

Serial Port Interface

The CS5525/26 serial interface consist of four pins, SCLK, SDO, SDI, and $\overline{CS}$. The $\overline{CS}$ pin must be held low (logic 0) before SCLK transitions can be recognized by the port logic. The SDO output will be held at high impedance any time $\overline{CS}$ is a logic 1.

If the $\overline{CS}$ pin is tied low, the port can function as a three wire interface.

The SCLK input is designed with a Schmitt-trigger input to allow an optoisolator with slower rise and fall times to directly drive the pin.

The SDO output is capable of sinking or sourcing up to 5 mA to directly drive an optoisolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcin g 5mA.

Serial Port Initialization

The serial port is initialized to the command mode whenever a power-on reset is performed inside the converter, when the port initialization sequence is completed, or whenever a command byte, data word sequence is completed. The port initialization sequence involves clocking 15 (or more) bytes of all 1's, followed by one byte with the following bit contents (11111110). This sequence places the chips in the command mode where it waits for a valid command.

Performing Conversions (With PF bit = 0)

Setting the SC (Single Conversion) bit of the command word to a logic 1 with the CB bit = 1, all other command bits = 0, the CS5525/CS5526 will perform one conversion. At the completion of the conversion the DF (Done Flag) bit of the configuration register will be set to a logic 1. The user can read the configuration register to determine if the DF bit is set. If DF has been set, a command can be issued to read the conversion data register to obtain the conversion data word. The DF bit of the configuration register will be cleared to logic 0 when the data register, the gain register, the offset register, or the set-up registers are read. Reading only the configuration register will not clear the DF flag bit.

If an SC command is issued to the converters while they are performing a conversion, the filter will restart a convolution cycle to perform a new conversion.

Performing Conversions (With PF bit = 1)

Setting the PF bit of the configuration register to a logic 1 enables the SDO output pin to behave as a flag signal whenever conversions are completed. This eliminates the need for the user to read the DF flag bit of the configuration register to determine if the conversion data word is available.

If the SC (Single Conversion) command is issued (SC = 1, CB= 1, all other command bits = 0) the SDO pin will go low at the completion of a conver-

sion. The user would then issue 8 SCLKs (with SDI = logic 0) to clear the SDO flag. Upon the falling edge of the 8th SCLK, the SDO pin will present the first bit (MSB) of the conversion word. 24 SCLKs (high, then low) are required to read the conversion word from the port. The user must not give an explicit command to read the conversion data register when the PF bit is set to logic 1. The data conversion word must be read before a new command can be entered (if the SC command is used with PF = 1).

If the CC (Continuous Conversion) command is issued (CC = 1, CB =1, all other command bits = 0) the SDO pin will go low at the completion of a conversion. The user would then issue 8 SCLKs (with SDI = logic 0) to clear the SDO flag. Upon the falling edge of the 8th SCLK, the SDO pin will present the first bit (MSB) of the conversion word. 24 SCLKs (high, then low) are required to read the conversion word from the port. The user must not give an explicit command to read the conversion data register when the PF bit is set to logic 1. When operating in the continuous conversion mode, the user need not read every conversion. If the user does nothing after SDO falls, SDO will rise one XIN clock cycle before the next conversion word is available and then fall again to signal that another conversion word is available. If the user begins to clear the SDO flag and read the conversion data, this action must be finished before the conversion cycle which is occurring in the background is complete if the user wants to be able to read the new conversion data.

To exit the continuous conversion mode, issue any valid command to the SDI input when the SDO flag falls. If a CC command is issued to the converter while it is performing a conversion, the filter will restart a convolution cycle to perform a new conversion.

Output Word Rate Selection

The WR2-WR0 bits of the configuration register set the output conversion word rate of the converters as shown in Table 2. The word rates indicated in the table assume a master clock of 32.768 kHz. Upon reset the converters are set to operate with an output word rate of 15.0 Hz.

Clock Generator

The CS5525/26 include a gate which can be connected with an external crystal to provide the master clock for the chips. They are designed to operate using a low-cost 32.768 kHz “tuning fork” type crystal. The 32.768 kHz crystal should be connected as shown in Figure 18. Lead lengths should be minimized to reduce stray capacitance.

The converters will operate with an external (CMOS compatible) clock with frequencies up to three times the typical crystal frequency of 32.768 kHz. Figure 17 details the converter’s performance at increased clock rates.

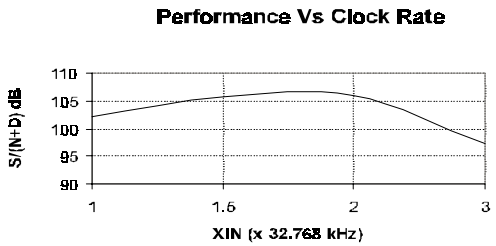


Figure 17. High Speed Clock Performance

The 32.768 kHz crystal is normally specified as a time-keeping crystal with tight specifications for both initial frequency and for drift over temperature. To maintain excellent frequency stability, these crystals are specified only over limited operating temperature ranges (i.e. -10 °C to +60 °C). However, applications with the CS5525/26 don’t generally require such tight tolerances. When 32.768 kHz tuning fork crystals are used, it is recommended that protection components, an external resistor and capacitor as shown in Figure 18, be used.

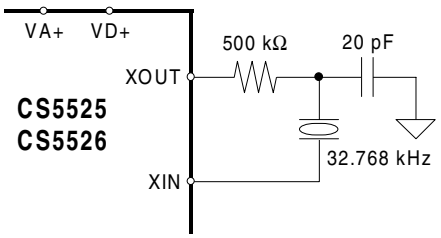


Figure 18. Tuning Fork Crystal Connection Diagram

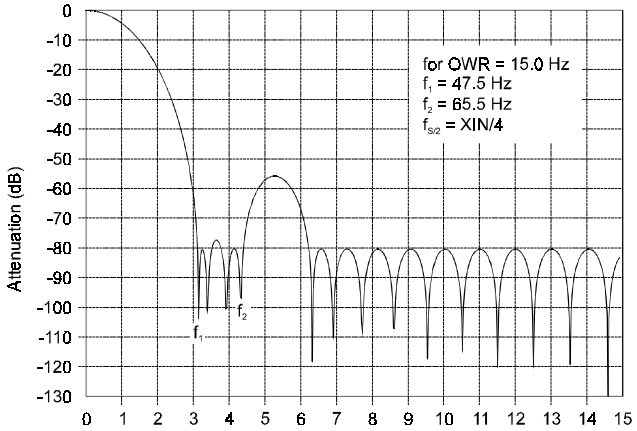


Figure 19. Filter Response
(Normalized to Output Word Rate = 1)

Digital Filter

The CS5525/26 have eight different linear phase digital filters which set the output word rates (OWRs) as stated in Table 2. These rates assume that XIN is 32.768 kHz. Each of the filters has a magnitude response similar to that shown in Figure 19. The filters are optimized to settle to full accuracy every conversion and yield better than 80 dB rejection for both 50 and 60 Hz with output word rates at or below 15.0 Hz.

The converter's digital filters scale with XIN. For example with an output word rate of 15 Hz, the filter's corner frequency is typically 12.7 Hz. If XIN is increased to 64.536 kHz the OWR doubles and the filter's corner frequency moves to 25.4 Hz.

Output Coding

The CS5525/26 output data in binary format when operating in unipolar mode and in two's complement when operating in bipolar mode.

The output conversion word is 24 bits, or three bytes long, as shown in Table 5. The MSB is output first followed by the rest of the data bits in descending order. For the CS5525 the last byte is composed of bits D7-D4, which are always logic 1; D3-D2, which are always logic 0; and bits D1-D0 which are the two flag bits. For the CS5526 the last byte includes data bits D7-D4, D3-D2 which are always logic 0 and the two flag bits.

The OF (Overrange Flag) bit is set to a logic 1 any time the input signal is: 1) more positive than positive full scale, 2) more negative than zero (unipolar mode), 3) more negative than negative full scale (bipolar mode). It is cleared back to logic 0 whenever a conversion word occurs which is not overranged.

The OD (Oscillation Detect) bit is set to a logic 1 any time that an oscillatory condition is detected in the modulator. This does not occur under normal operating conditions, but may occur whenever the input

Output Conversion Data CS5525 (16 bits + flags)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB	1	1	1	1	0	0	OD	OF

Output Conversion Data CS5526 (20 bits + flags)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB	0	0	OD	OF

Table 5. Data Conversion Word

CS5525 16-Bit Output Coding			
Unipolar Input Voltage	Offset Binary	Bipolar Input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFF	>(VFS-1.5 LSB)	7FFF
VFS-1.5 LSB	FFFF ----- FFFE	VFS-1.5 LSB	7FFF ----- 7FFE
VFS/2-0.5 LSB	8000 ----- 7FFF	-0.5 LSB	0000 ----- FFFF
+0.5 LSB	0001 ----- 0000	-VFS+0.5 LSB	8001 ----- 8000
<(+0.5 LSB)	0000	<(-VFS+0.5 LSB)	8000

CS5526 20-Bit Output Coding			
Unipolar Input Voltage	Offset Binary	Bipolar Input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFFF	>(VFS-1.5 LSB)	7FFFF
VFS-1.5 LSB	FFFFF ----- FFFFE	VFS-1.5 LSB	7FFFF ----- 7FFFE
VFS/2-0.5 LSB	80000 ----- 7FFFF	-0.5 LSB	00000 ----- FFFFF
+0.5 LSB	00001 ----- 00000	-VFS+0.5 LSB	80001 ----- 80000
<(+0.5 LSB)	00000	<(-VFS+0.5 LSB)	80000

Note: VFS in the table equals the voltage between ground and full scale for any of the unipolar gain ranges, or the voltage between ± full scale for any of the bipolar gain ranges. See text about error flags under overrange conditions.

Table 6. 5525/26 Output Coding

to the converters is extremely overranged. If the OD bit is set, the conversion data bits can be completely erroneous. The OD flag bit will be cleared to logic 0 when the modulator becomes stable. Table 6 illustrates the output coding for the CS5525/26.

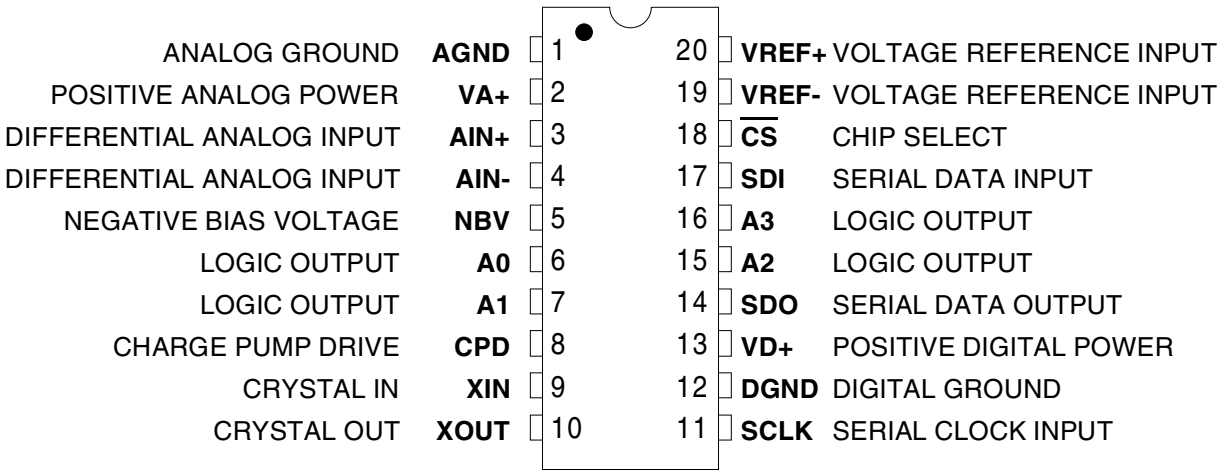
Power Consumption

The CS5525/26 accommodate four power consumption modes: normal, low power, standby, and sleep. The normal mode, the default mode, is entered after a power-on-reset and typically consumes 9.4 mW. The low power mode is an alternate mode that reduces the consumed power to 4.9 mW. It is entered by setting bit D16 (the low power mode bit) in the configuration register to logic 1. Since the converter's noise performance improves with increased power consumption, slightly degraded noise or linearity performance should be expected in the low power mode. The final two modes are referred to as the power save modes. They power down most of the analog portion of the chips and stop filter convolutions. The power save modes are entered whenever the PS/$\overline{R}$ bit and the CB bit of the command word are set to logic 1. The particular power save mode entered depends on state of bit D4 (the Power Save Select bit) in the configuration register. If D4 is logic 0, the converters enters the standby mode reducing the power consumption to 1.2mW. The standby mode leaves the oscillator and the on-chip bias generator running. This allows the converters to quickly return to the normal or low power mode once the PS/$\overline{R}$ bit is set back to a logic 1. If D4 in the configuration register and CB and PS/$\overline{R}$ in the command word are set to logic 1, the sleep mode is entered reducing the consumed power to less than 500 µW. Since the sleep mode disables the oscillator, approximately a 500ms oscillator start-up delay period is required before returning to the normal or low power mode.

PCB Layout

The CS5525/26 should be placed entirely over an analog ground plane with both the AGND and DGND pins of the device connected to the analog plane. Place the analog-digital plane split immediately adjacent to the digital portion of the chip.

PIN DESCRIPTIONS



Clock Generator

XIN; XOUT - Crystal In; Crystal Out, Pins 9, 10.

A gate inside the chip is connected to these pins and can be used with a crystal to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be supplied into the XIN pin to provide the master clock for the device.

Control Pins and Serial Data I/O

$\overline{\text{CS}}$ - Chip Select, Pin 18.

When active low, the port will recognize SCLK. When high the SDO pin will output a high impedance state. $\overline{\text{CS}}$ should be changed when SCLK = 0.

SDI - Serial Data Input, Pin 17.

SDI is the input pin of the serial input port. Data will be input at a rate determined by SCLK.

SDO - Serial Data Output, Pin 14.

SDO is the serial data output. It will output a high impedance state if $\overline{\text{CS}}$ = 1.

SCLK - Serial Clock Input, Pin 11.

A clock signal on this pin determines the input/output rate of the data for the SDI/SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{\text{CS}}$ is low.

A0, A1, A2, A3 - Logic Outputs, Pin 6, 7, 15, 16.

The logic states of A0-A3 mimic the states of the D20-D23 bits of the configuration register. Logic Output 0 = AGND, and Logic Output 1 = VA+.

Measurement and Reference Inputs

AIN+, AIN- - Differential Analog Input, Pins 3, 4.

Differential input pins into the device.

VREF+, VREF- - Voltage Reference Input, Pins 20, 19.

Fully differential inputs which establish the voltage reference for the on-chip modulator.

NBV - Negative Bias Voltage, Pin 5.

Input pin to supply the negative supply voltage for the 20X gain instrumentation amplifier. May be tied to AGND if AIN+ and AIN- inputs are centered around +2.5 V; or it may be tied to a negative supply voltage (-2.1 V typical) to allow the amplifier to handle low level signals more negative than ground.

CPD - Charge Pump Drive, Pin 8.

Square wave output used to provide energy for the charge pump.

Power Supply Connections

VA+ - Positive Analog Power, Pin 2.

Positive analog supply voltage. Nominally +5 V.

VD+ - Positive Digital Power, Pin 13.

Positive digital supply voltage. Nominally +3.0 V or +5 V.

AGND - Analog Ground, Pin 1.

Analog Ground.

DGND - Digital Ground, Pin 12.

Digital Ground.

SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

Full Scale Error

The deviation of the last code transition from the ideal [{(VREF+) - (VREF-)} - 3/2 LSB]. Units are in LSBs.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above the voltage on the AIN- pin.). When in unipolar mode ($U/\overline{B}$ bit = 1). Units are in LSBs.

Bipolar Offset

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below the voltage on the AIN- pin). When in bipolar mode ($U/\overline{B}$ bit = 0). Units are in LSBs.

ORDERING GUIDE

Model Number	Linearity Error (Max)	Temperature Range	Package
CS5525-AP	±0.003%	-40°C to +85°C	20-pin 0.3" Plastic DIP
CS5525-AS	±0.003%	-40°C to +85°C	20-pin 0.2" Plastic SSOP
CS5526-BP	±0.0015%	-40°C to +85°C	20-pin 0.3" Plastic DIP
CS5526-BS	±0.0015%	-40°C to +85°C	20-pin 0.2" Plastic SSOP

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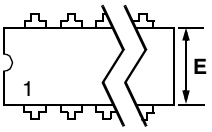
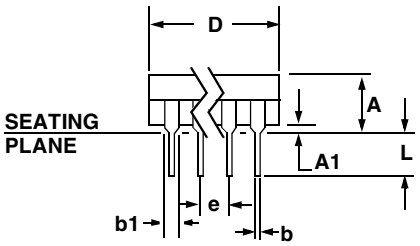
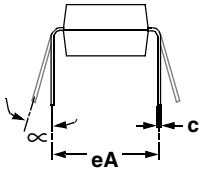
20 PIN PLASTIC (PDIP) PACKAGE DRAWING



TOP VIEW



BOTTOM VIEW



SIDE VIEW

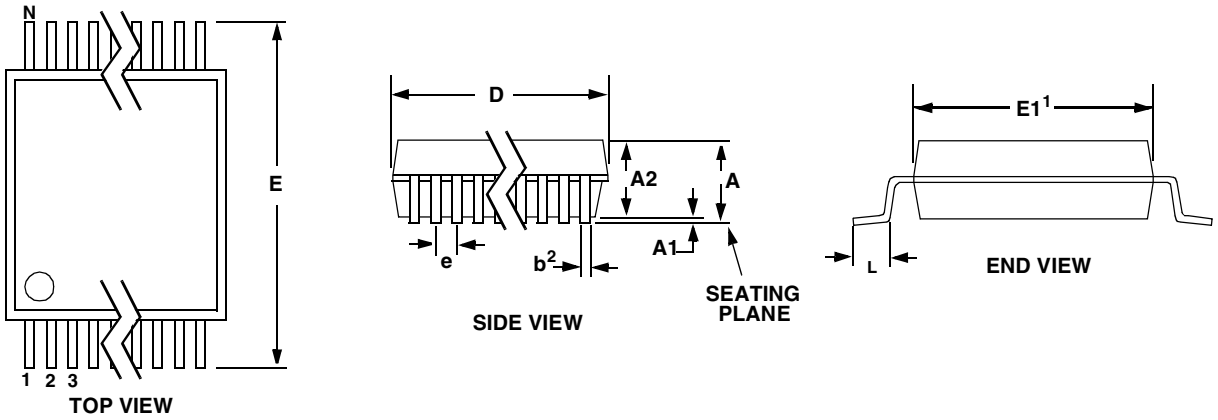
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.155	0.180	3.94	4.57
A1	0.020	0.040	0.51	1.02
b	0.015	0.022	0.38	0.56
b1	0.050	0.065	1.27	1.65
c	0.008	0.015	0.20	0.38
D	0.960	1.040	24.38	26.42
E	0.240	0.260	6.10	6.60
e	0.095	0.105	2.41	2.67
eA	0.300	0.325	7.62	8.25
L	0.125	0.150	3.18	3.81
∝	0°	15°	0°	15°

Notes: 1. Positional tolerance of leads shall be within 0 .25mm (0. 010in.) at maximum material condition, in relation to seating plane and each other.

2. Dimension eA to center of leads when formed parallel.

3. Dimension E does not include mold flash.

20 PIN SSOP PACKAGE DRAWING



	INCHES		MILLIMETERS		NOTE
DIM	MIN	MAX	MIN	MAX	
A	--	0.084	--	2.13	
A1	0.002	0.010	0.05	0.25	
A2	0.064	0.074	1.62	1.88	
b	0.009	0.015	0.22	0.38	2,3
D	0.272	0.295	6.90	7.50	1
E	0.291	0.323	7.40	8.20	
E1	0.197	0.220	5.00	5.60	1
e	0.024	0.027	0.61	0.69	
L	0.025	0.040	0.63	1.03	
∝	0°	8°	0°	8°	

Notes: 1. “D” and “E1” are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension “b” does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of “b” dimension at maximum material condition. Dambar intrusion shall not reduce dimension “b” by more than 0.0 7mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 a nd 0.25mm from lead tips.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com**