NEC

# MOS FIELD EFFECT TRANSISTOR

# μPA1759

## SWITCHING
## N-CHANNEL POWER MOS FET
## INDUSTRIAL USE

### DESCRIPTION

This product is Dual N-channel MOS Field Effect Transistor designed for DC/DC converters.

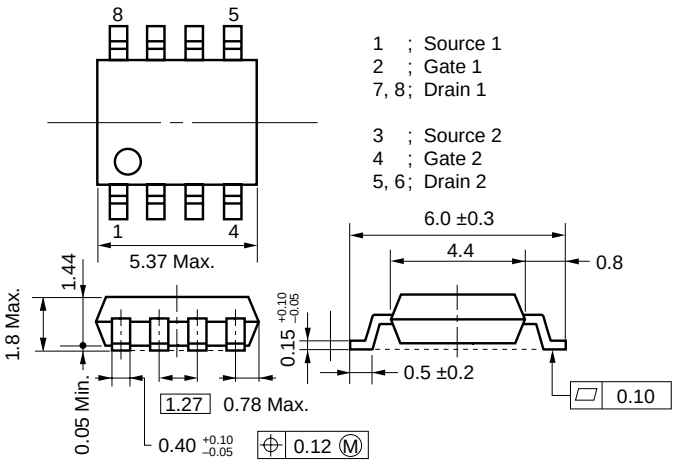
### FEATURES

- Dual chip type
- Low on-resistance
  $R_{DS(on)1}$ = 110 mΩ TYP. ($V_{GS}$ = 10 V, $I_D$ = 2.5 A)
  $R_{DS(on)2}$ = 170 mΩ TYP. ($V_{GS}$ = 4 V, $I_D$ = 2.5 A)
- Low input capacitance $C_{iss}$ = 190 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

### ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| μPA1759G | Power SOP8 |

### PACKAGE DRAWING (Unit : mm)

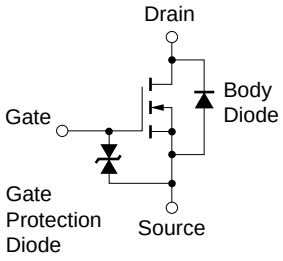



### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, All terminals are connected.)

| | | | |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS}$ = 0) | $V_{DSS}$ | 60 | V |
| Gate to Source Voltage ($V_{DS}$ = 0) | $V_{GSS}$ | ±20 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ±5.0 | A |
| Drain Current (pulse) Note1 | $I_{D(pulse)}$ | ±20 | A |
| Total Power Dissipation (1 unit) Note2 | $P_T$ | 1.7 | W |
| Total Power Dissipation (2 unit) Note2 | $P_T$ | 2.0 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | –55 to + 150 | °C |
| Single Avalanche Current Note3 | $I_{AS}$ | 2.5 | A |
| Single Avalanche Energy Note3 | $E_{AS}$ | 0.625 | mJ |

### EQUIVALENT CIRCUIT

(1/2 Circuit)




**Notes 1.** PW ≤ 10 μs, Duty cycle ≤ 1 %

**2.** Mounted on ceramic substrate of 1200 $mm^2$ x 1.7 mm

**3.** Starting $T_{ch}$ = 25 °C, $R_G$ = 25 Ω, $V_{GS}$ = 20 V → 0 V

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.



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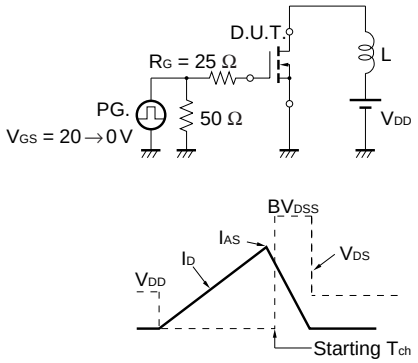
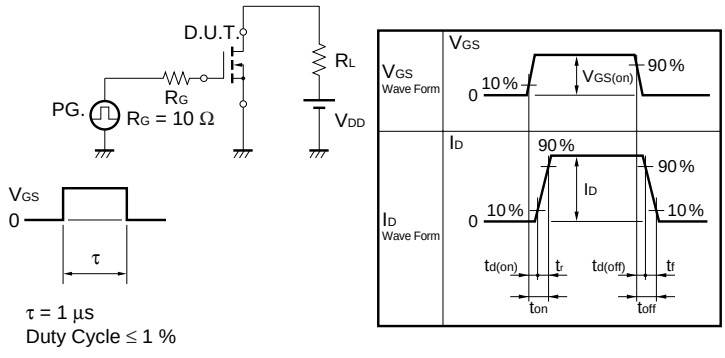
## ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C, All terminals are connected.)

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Drain to Source On-state Resistance | $R_{DS(on)1}$ | $V_{GS}$ = 10 V, $I_D$ = 2.5 A | | 110 | 150 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = 4 V, $I_D$ = 2.5 A | | 170 | 240 | mΩ |
| Gate to Source Cut-off Voltage | $V_{GS(off)}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 1.0 | 1.7 | 2.5 | V |
| Forward Transfer Admittance | $\|y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 2.5 A | 2.0 | 3.9 | | S |
| Drain Leakage Current | $I_{DSS}$ | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | | | 10 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V | | 190 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | | 100 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 36 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $I_D$ = 2.5 A | | 6 | | ns |
| Rise Time | $t_r$ | $V_{GS(on)}$ = 10 V | | 50 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $V_{DD}$ = 15 V | | 80 | | ns |
| Fall Time | $t_f$ | $R_G$ = 10 Ω | | 50 | | ns |
| Total Gate Charge | $Q_G$ | $I_D$ = 5.0 A | | 8 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{DD}$ = 24 V | | 1 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $V_{GS}$ = 10 V | | 2.4 | | nC |
| Body Diode forward Voltage | $V_{F(S-D)}$ | $I_F$ = 5.0 A, $V_{GS}$ = 0 V | | 0.9 | | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 5.0 A, $V_{GS}$ = 0 V | | 40 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100 A/μs | | 50 | | nC |

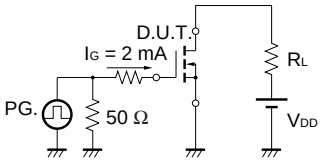
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**




**TEST CIRCUIT 2 SWITCHING TIME**




**TEST CIRCUIT 3 GATE CHARGE**



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