MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

Advance Information

MC68230

PARALLEL INTERFACE/TIMER (PI/T)

DECEMBER, 1983

TABLE OF CONTENTS

TABLE OF CONTENTS
(Continued)

TABLE OF CONTENTS
(Concluded)

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1
INTRODUCTION

The MC68230 parallel interface/timer (PI/T) provides versatile double buffered parallel interfaces and a system oriented timer for M68000 systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8 or 16 bits wide. In the unidirectional modes, an associated data direction register determines whether each port pin is an input or output. In the bidirectional modes the data direction registers are ignored and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high speed peripherals or other computer systems. The PI/T ports allow use of vectored or autovectored interrupts, and also provide a DMA request pin for connection to the MC68450 direct memory access controller (DMAC) or a similar circuit. The PI/T timer contains a 24-bit wide counter and a 5-bit prescaler. The timer may be clocked by the system clock (PI/T CLK pin) or by an external clock (TIN pin), and a 5-bit prescaler can be used. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. It can also be used for elapsed time measurement or as a device watchdog.

Features of the PI/T include:

- M68000 Bus Compatible
- Port Modes Include:
  - Bit I/O
  - Unidirectional 8 Bit and 16 Bit
  - Bidirectional 8 Bit and 16 Bit
- Programmable Handshaking Options
- 24-Bit Programmable Timer Modes
- Five Separate Interrupt Vectors
- Separate Port and Timer Interrupt Service Requests
- Registers are Read/Write and Directly Addressable
- Registers are Addressed for MOVEP (Move Peripheral) and DMAC Compatibility

The PI/T consists of two logically independent sections: the ports and the timer. The port section consists of port A (PA0-PA7), port B (PB0-PB7), four handshake pins (H1, H2, H3, and H4), two general input/output (I/O) pins, and six dual-function pins. The dual-function pins can individually operate as a third port (port C) or an alternate function related to either port A, port B, or the timer. The four programmable handshake pins, depending on the mode, can control data transfer to and from the ports, or can be used as interrupt generating inputs or I/O pins. Refer to Figure 1-1.

The timer consists of a 24-bit counter, optionally clocked by a 5-bit prescaler. Three pins provide complete timer I/O: PC2/TIN, PC3/TOUT, and PC7/$\overline{\text{TIACK}}$. Only the ones needed for the given configuration perform the timer function, while the others remain port C I/O.

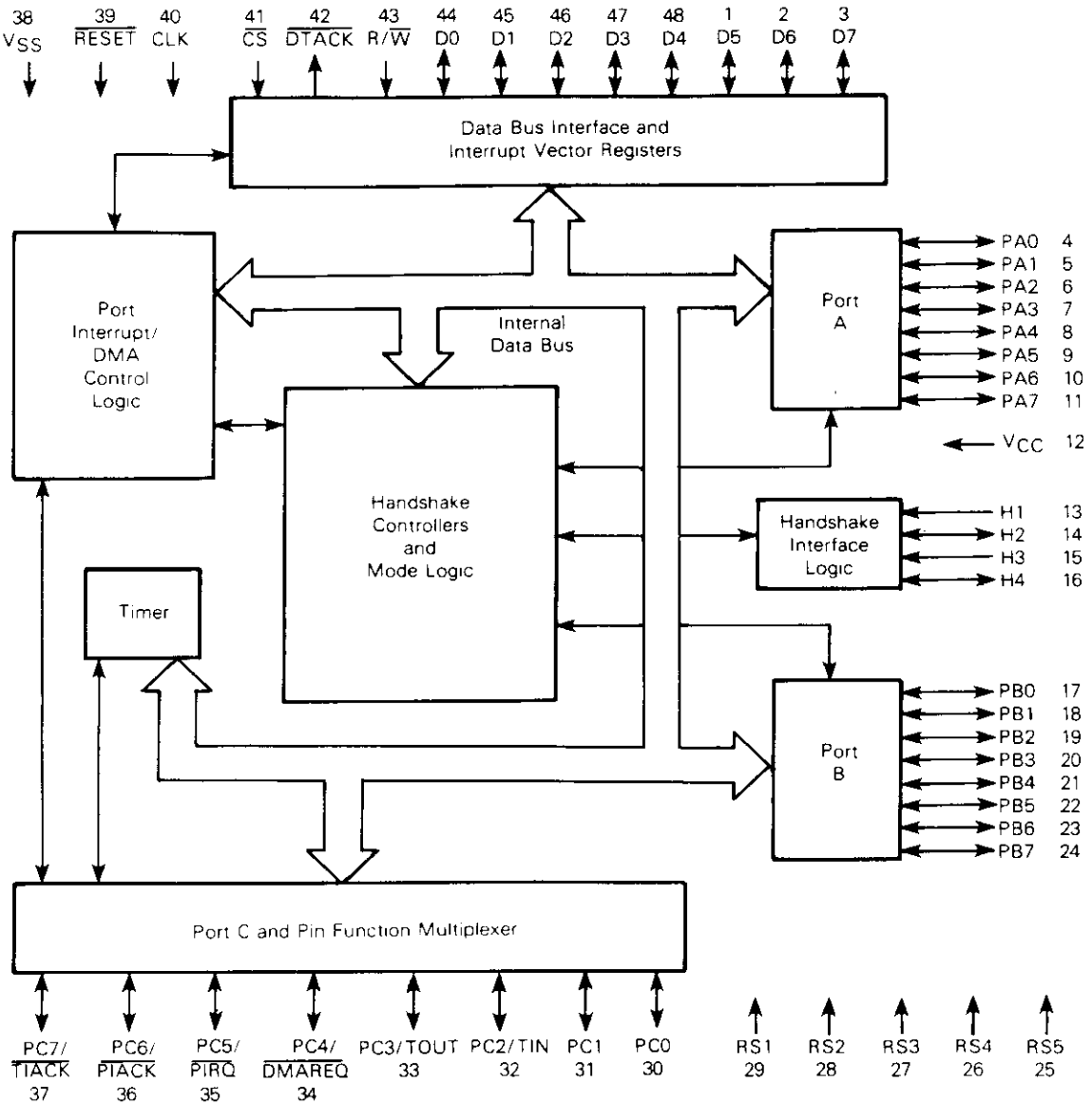


Figure 1-1. Block Diagram

The system bus interface provides for asynchronous transfer of data from the PI/T to a bus master over the data bus (D0-D7). Data transfer acknowledge ($\overline{DTACK}$), register selects (RS1-RS5), timer interrupt acknowledge ($\overline{TIACK}$), read/write line (R/$\overline{W}$), chip select ($\overline{CS}$), or port interrupt acknowledge ($\overline{PIACK}$) control data transfer between the PI/T and an M68000.

1.1 PORT MODE DESCRIPTION

The primary focus of most applications will be on port A, port B, the handshake pins, the port interrupt pins, and the DMA request pin. They are controlled in the following way: the port general control register contains a 2-bit field that specifies one of four operation modes. These govern the

overall operation of the ports and determine their interrelationships. Some modes require additional information from each port's control register to further define its operation. In each port control register, there is a 2-bit submode field that serves this purpose. Each port mode/submode combination specifies a set of programmable characteristics that fully define the behavior of that port and two of the handshake pins. This structure is summarized in Table 1-1 and Figure 1-2.

Table 1-1. Port Mode Control Summary

Mode 0 (Unidirectional 8-Bit Mode)
- Port A
  - Submode 00 – Pin-Definable Double-Buffered Input or Single-Buffered Output
    - H1 – Latches input data
    - H2 – Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed handshake protocols
  - Submode 01 – Pin-Definable Double-Buffered Output or Non-Latched Input
    - H1 – Indicates data received by peripheral
    - H2 – Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed handshake protocols
  - Submode 1X – Pin-Definable Single-Buffered Output or Non-Latched Input
    - H1 – Status/interrupt generating input
    - H2 – Status/interrupt generating input or general-purpose output
- Port B
  - H3 and H4 – Identical to port A, H1 and H2

Mode 1 (Unidirectional 16-Bit Mode)
- Port A – Most-Significant Data Byte or Non-Latched Input or Single-Buffered Output
  - Submode XX – (not used)
    - H1 – Status/interrupt generating input
    - H2 – Status/interrupt generating input or general-purpose output
- Port B – Least-Significant Data Byte
  - Submode X0 – Pin-Definable Double-Buffered Input or Single-Buffered Output
    - H3 – Latches input data
    - H4 – Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed handshake protocols
  - Submode X1 – Pin-Definable Double-Buffered Output or Non-Latched Input
    - H3 – Indicates data received by peripheral
    - H4 – Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed handshake protocols

Mode 2 (Bidirectional 8-Bit Mode)
- Port A – Bit I/O
  - Submode XX – (not used)
- Port B – Double-Buffered Bidirectional Data
  - Submode XX – (not used)
    - H1 – Indicates output data received by the peripheral and controls output drivers
    - H2 – Operation with H1 in the interlocked or pulsed output handshake protocols
    - H3 – Latches input data
    - H4 – Operation with H3 in the interlocked or pulsed input handshake protocols

Mode 3 (Bidirectional 16-Bit Mode)
- Port A – Double-Buffered Bidirectional Data (Most-Significant Data Byte)
  - Submode XX – (not used)
- Port B – Double-Buffered Bidirectional Data (Least-Significant Data Byte)
  - Submode XX – (not used)
    - H1 – Indicates output data received by peripheral and controls output drivers
    - H2 – Operation with H1 in the interlocked or pulsed output handshake protocols
    - H3 – Latches input data
    - H4 – Operation with H3 in the interlocked or pulsed input handshake protocols

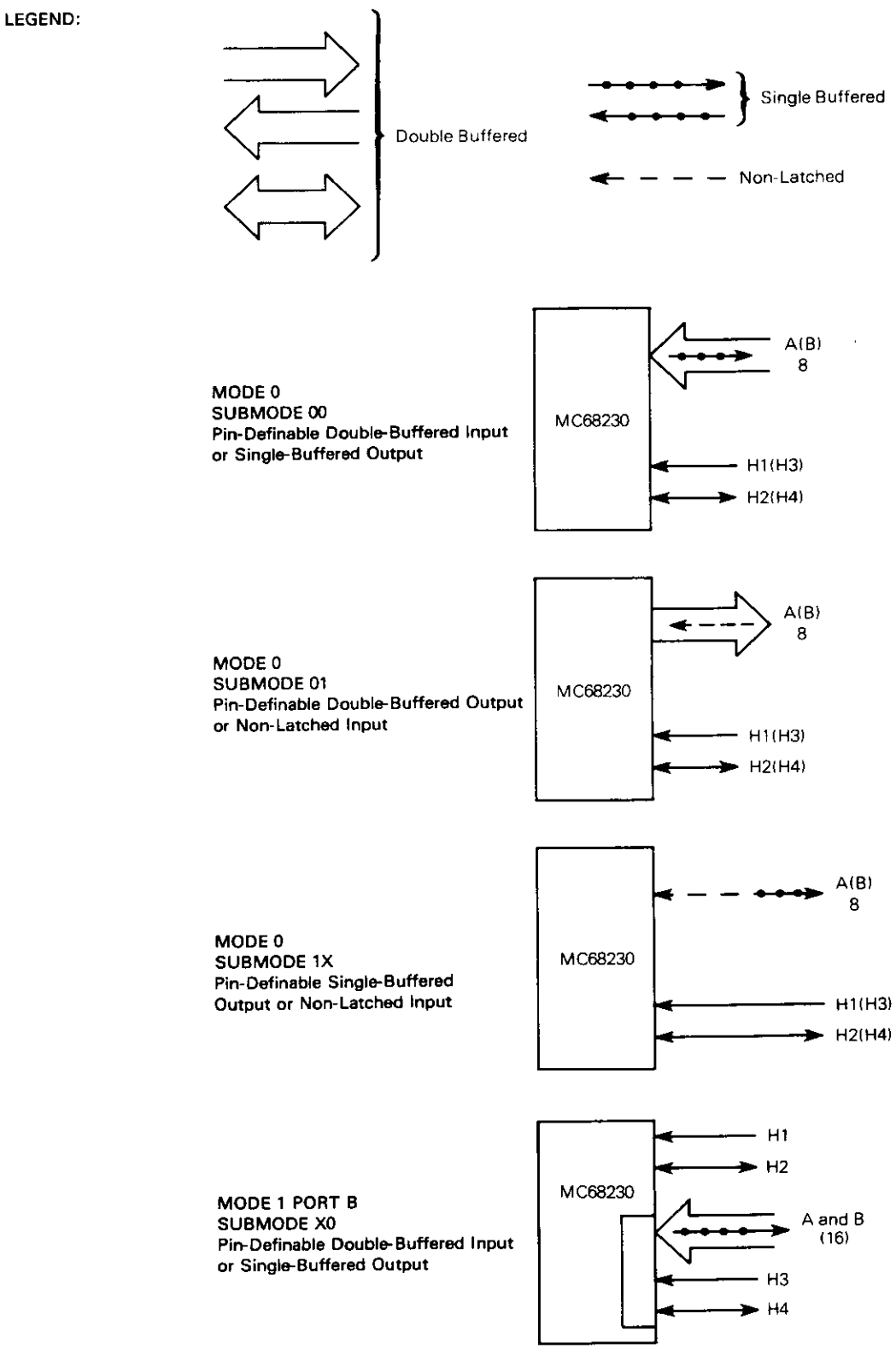


Figure 1-2. Port Mode Layout (Sheet 1 of 2)

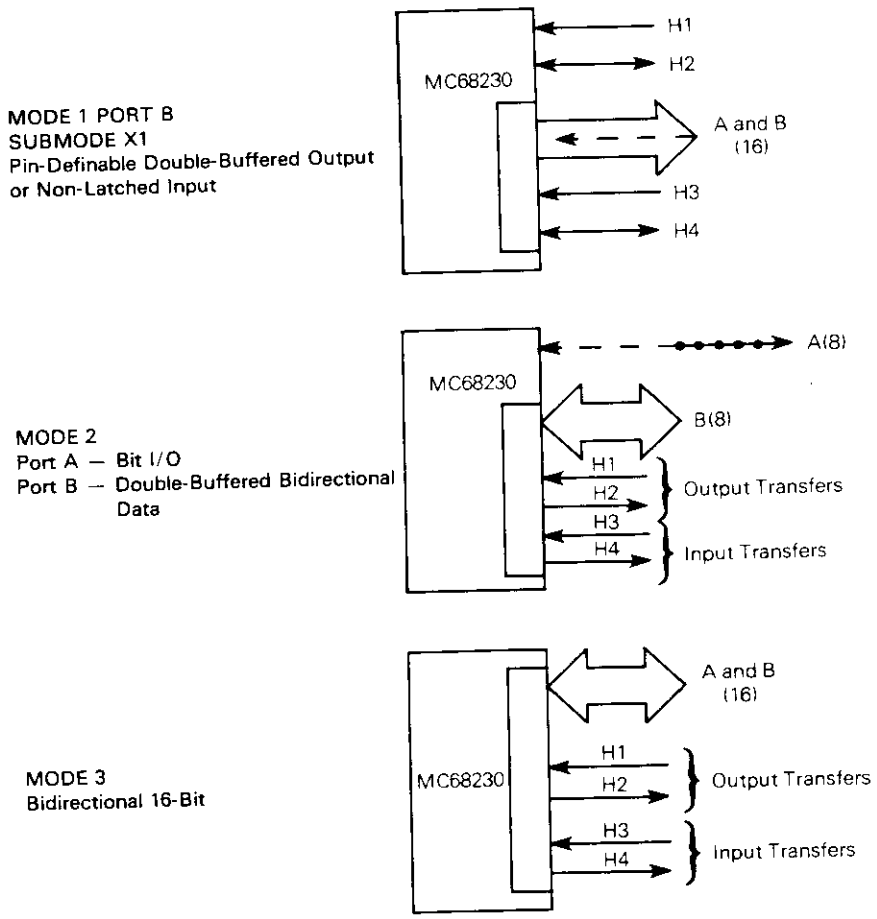


Figure 1-2. Port Mode Layout (Sheet 2 of 2)

1.2 SIGNAL DESCRIPTION

Throughout this data sheet, signals are presented using the terms active and inactive or asserted and negated independent or whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is given below.) Active low signals are denoted by a superscript bar. R/$\overline{W}$ indicates a write is active low and a read active high. Table 1-2 further describes each pin and the logical pin assignments are given in Figure 1-3.

1.2.1 Bidirectional Data Bus (D0-D7)

The data bus pins, D0-D7, form an 8-bit bidirectional data bus to/from an M68000 bus master. These pins are active high.

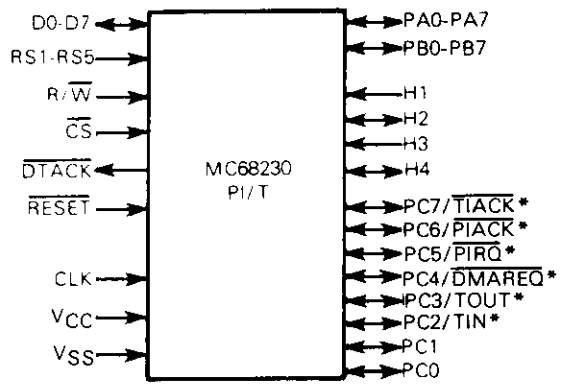
1.2.2 Register Selects (RS1-RS5)

The register select pins, RS1-RS5, are active high high-impedance inputs that determine which of the 23 internal registers is being selected. They are provided by the M68000 bus master or other bus master.

Table 1-2. Signal Summary

Signal Name	Input/Output	Active State	Edge/Level Sensitive	Output States
CLK	Input		Falling and Rising Edge	
$\overline{CS}$	Input	Low	Level	
D0-D7	Input/Output	High = 1, Low = 0	Level	High, Low, High Impedance
$\overline{DMAREQ}$	Output	Low		High, Low
$\overline{DTACK}$	Output	Low		High, Low, High Impedance*
H1(H3)***	Input	Low or High	Asserted Edge	
H2(H4)**	Input or Output	Low or High	Asserted Edge	High, Low, High Impedance
PA0-PA7**, PB0-PB7**, PC0-PC7	Input/Output, Input or Output	High = 1, Low = 0	Level	High, Low, High Impedance
$\overline{PIACK}$	Input	Low	Level	
$\overline{PIRQ}$	Output	Low		Low, High Impedance*
RS1-RS5	Input	High = 1, Low = 0	Level	
R/$\overline{W}$	Input	High Read, Low Write	Level	
$\overline{RESET}$	Input	Low	Level	
$\overline{TIACK}$	Input	Low	Level	
TIN (External Clock)	Input		Rising Edge	
TIN (Run/Halt)	Input	High	Level	
TOUT (Square Wave)	Output	Low		High, Low
TOUT ($\overline{TIRQ}$)	Output	Low		Low, High Impedance*

* Pullup resistors required.
** Note these pins have internal pullup resistors.
*** H1 is level sensitive for output buffer control in modes 2 and 3.



* Individually Programmable Dual-Function Pin

Figure 1-3. Logical Pin Assignment

1.2.3 Read/Write (R/$\overline{W}$)

R/$\overline{W}$ is a high-impedance read/write input signal from the M68000 bus master, indicating whether the current bus cycle is a read (high) or write (low) cycle.

1.2.4 Chip Select ($\overline{CS}$)

$\overline{CS}$ is a high-impedance input that selects the PI/T registers for the current bus cycle. Address strobe and the data strobe (upper or lower) of the bus master, along with the appropriate address bits, must be included in the chip-select equation. A low level corresponds to an asserted chip select.

1.2.5 Data Transfer Acknowledge ($\overline{DTACK}$)

$\overline{DTACK}$ is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. Data transfer acknowledge is compatible with the MC68000 and with other M68000 bus masters such as the MC68450 direct memory access controller (DMAC). A pullup resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

1.2.6 Reset ($\overline{RESET}$)

$\overline{RESET}$ is a high-impedance input used to initialize all PI/T functions. All control and data direction registers are cleared and most internal operations are disabled by the assertion of $\overline{RESET}$ (low).

1.2.7 Clock (CLK)

The clock pin is a high-impedance TTL-compatible signal with the same specifications as the MC68000. The PI/T contains dynamic logic throughout, and hence this clock must not be gated off at any time. It is not necessary that this clock maintain any particular phase relationship with the M68000 system clock. It may be connected to an independent frequency source (faster or slower) as long as all bus specifications are met.

1.2.8 Port A and Port B (PA0-PA7 and PB0-PB7)

Ports A and B are 8-bit ports that may be concatenated to form a 16-bit port in certain modes. The ports may be controlled in conjunction with the handshake pins H1-H4. For stabilization during system power up, ports A and B have internal pullup resistors to V_{CC}. All port pins are active high.

1.2.9 Handshake Pins (H1-H4)

Handshake pins H1-H4 are multi-purpose pins that (depending on the operational mode) may provide an interlocked handshake, a pulsed handshake, an interrupt input (independent of data transfers), or simple I/O pins. For stabilization during system power up, H2 and H4 have internal pullup resistors to V_{CC}. The sense of H1-H4 (active high or low) may be programmed in the port general control register bits 3-0. Independent of the mode, the instantaneous level of the handshake pins can be read from the port status register.

1.2.10 Port C (PC0-PC7/Alternate Function)

This port can be used as eight general purpose I/O pins (PC0-PC7) or any combination of six special function pins and two general purpose I/O pins (PC0-PC1). Each dual-function pin can be a standard I/O or a special function independent of the other port C pins. When used as a port C pin, these pins are active high. They may be individually programmed as inputs or outputs by the port C data direction register. The dual-function pins are defined in the following paragraphs.

The alternate functions TIN, TOUT, and $\overline{TIACK}$ are timer I/O pins. TIN may be used as a rising-edge triggered external clock input or an external run/halt control pin (the timer is in the run state if run/halt is high and in the halt state if run/halt is low). TOUT may provide an active low timer interrupt request output or a general-purpose square-wave output, initially high. $\overline{TIACK}$ is an active low high-impedance input used for timer interrupt acknowledge.

Port A and B functions have an independent pair of active low interrupt request ($\overline{PIRQ}$) and interrupt acknowledge ($\overline{PIACK}$) pins.

The $\overline{DMAREQ}$ (direct memory access request) pin provides an active low direct memory access controller request pulse for three clock cycles, completely compatible with the MC68450 DMAC.

1.3 REGISTER MODEL

A register model that includes the corresponding register selects is shown in Table 1-3.

Table 1-3. Register Model (Sheet 1 of 2)

Register Select Bits 5	4	3	2	1	7	6	5	4	3	2	1	0	Register Value After $\overline{RESET}$ (Hex Value)	
0	0	0	0	0	Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense	0 0	Port General Contol Register
0	0	0	0	1	*	SVCRQ Select		IPF Select		Port Interrupt Priority Control			0 0	Port Service Request Register
0	0	0	1	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port A Data Direction Register
0	0	0	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port B Data Direction Register
0	0	1	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port C Data Direction Register
0	0	1	0	1	Interrupt Vector Number						*	*	0 F	Port Interrupt Vector Register
0	0	1	1	0	Port A Submode		H2 Control			H2 Int Enable	H1 SVCRQ Enable	H1 Stat Ctrl	0 0	Port A Control Register
0	0	1	1	1	Port B Submode		H4 Control			H4 Int Enable	H3 SVCRQ Enable	H3 Stat Ctrl	0 0	Port B Control Register
0	1	0	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Port A Data Register
0	1	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Port B Data Register
0	1	0	1	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	***	Port A Alternate Register
0	1	0	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	***	Port B Alternate Register
0	1	1	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	****	Port C Data Register
0	1	1	0	1	H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S	****	Port Status Register
0	1	1	1	0	*	*	*	*	*	*	*	*	0 0	(Null)
0	1	1	1	1	*	*	*	*	*	*	*	*	0 0	(Null)

* Unused, read as zero
** Value before $\overline{RESET}$
*** Current value on pins
**** Undetermined value

Table 1-3. Register Model (Sheet 2 of 2)

Register Select Bits 5	4	3	2	1	7	6	5	4	3	2	1	0	Register Value After $\overline{\text{RESET}}$ (Hex Value)	
1	0	0	0	0	TOUT/$\overline{\text{TIACK}}$ Control			Z D Ctrl	*	Clock Control		Timer Enable	0 0	Timer Control Register
1	0	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 F	Timer Interrupt Vector Register
1	0	0	1	0	*	*	*	*	*	*	*	*	0 0	(Null)
1	0	0	1	1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	* *	Counter Preload Register (High)
1	0	1	0	0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	* *	Counter Preload Register (Mid)
1	0	1	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	* *	Counter Preload Register (Low)
1	0	1	1	0	*	*	*	*	*	*	*	*	0 0	(Null)
1	0	1	1	1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	* *	Count Register (High)
1	1	0	0	0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	* *	Count Register (Mid)
1	1	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	* *	Count Register (Low)
1	1	0	1	0	*	*	*	*	*	*	*	ZDS	0 0	Timer Status Register
1	1	0	1	1	*	*	*	*	*	*	*	*	0 0	(Null)
1	1	1	0	0	*	*	*	*	*	*	*	*	0 0	(Null)
1	1	1	0	1	*	*	*	*	*	*	*	*	0 0	(Null)
1	1	1	1	0	*	*	*	*	*	*	*	*	0 0	(Null)
1	1	1	1	1	*	*	*	*	*	*	*	*	0 0	(Null)

* Unused, read as zero
* * Value before $\overline{\text{RESET}}$

NOTE

Table 1-3 has been duplicated on foldout pages 1 and 2 at the end of this document for your convenience.

1.4 BUS INTERFACE OPERATION

The PI/T has an asynchronous bus interface, primarily designed for use with an M68000 microprocessor. With care, however, it can be connected to synchronous microprocessor buses. This section completely describes the PI/T's bus interface, and is intended for the asynchronous bus designer unless otherwise mentioned.

In an asynchronous system the PI/T clock may operate at a significantly different frequency, either higher or lower, than the bus master and other system components, as long as all bus specifications are met. The MC68230 CLK pin has the same specifications as the MC68000 CLK pin, and must not be gated off at any time.

The following signals generate normal read and write cycles to the PI/T: $\overline{CS}$ (chip select), R/$\overline{W}$ (read/write), RS1-RS5 (five register select bits), D0-D7 (the 8-bit bidirectional data bus), and $\overline{DTACK}$ (data transfer acknowledge). To generate interrupt acknowledge cycles, PC6/$\overline{PIACK}$ or PC7/$\overline{TIACK}$ is used instead of $\overline{CS}$, and the register select pins are ignored. No combination of the following pin functions may be asserted simultaneously: $\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$.

1.4.1 Read Cycles

This category includes all register reads, except port or timer interrupt acknowledge cycles. When $\overline{CS}$ is asserted, the register select and R/$\overline{W}$ inputs are latched internally. They must meet small setup and hold time requirements with respect to the asserted edge of $\overline{CS}$. (Refer to **6.6 AC ELECTRICAL SPECIFICATIONS** for further information.) The PI/T is **not** protected against aborted (shortened) bus cycles generated by an address error or bus error exception in which it is addressed.

Certain operations triggered by normal read (or write) bus cycles are not complete within the time allotted to the bus cycle. One example is transfers to/from the double-buffered latches that occur as a result of the bus cycle. If the bus master's clock is significantly faster than the PI/T's the possibility exists that, following the bus cycle, $\overline{CS}$ can be negated then re-asserted before completion of these internal operations. In this situation the PI/T does not recognize the re-assertion of $\overline{CS}$ until these operations are complete. Only at that time does it begin the internal sequencing necessary to react to the asserted $\overline{CS}$. Since $\overline{CS}$ also controls the $\overline{DTACK}$ response, this "bus cycle recovery time" can be related to the clock edge on which $\overline{DTACK}$ is asserted for that cycle. The PI/T will recognize the subsequent assertion of $\overline{CS}$ three clock periods after the clock edge on which $\overline{DTACK}$ was previously asserted.

The register select and R/$\overline{W}$ inputs pass through an internal latch that is transparent when the PI/T can recognize a new $\overline{CS}$ pulse (see above paragraph). Since the internal data bus of the PI/T is continuously engaged for read transfers, the read access time (to the data bus buffers) begins when the register selects are stabilized internally. Also, when the PI/T is ready to begin a new bus cycle, the assertion of $\overline{CS}$ enables the data bus buffers within a short propagation delay. This does not contribute to the overall read access time unless $\overline{CS}$ is asserted significantly after the register select and R/$\overline{W}$ inputs are stabilized (as may occur with synchronous bus microprocessors).

In addition to the chip select's previously mentioned duties, it controls the assertion of $\overline{DTACK}$ and latching of read data at the data bus interface. Except for controlling input latches and enabling the data bus buffers, all of these functions occur only after $\overline{CS}$ has been recognized internally and synchronized with the internal clock. Chip select is recognized on the falling edge of the clock if the setup time is met; $\overline{DTACK}$ is asserted (low) on the next falling edge of the clock. Read data is

latched at the PI/T's data bus interface at the same time $\overline{DTACK}$ is asserted. It is stable as long as chip select remains asserted independent of other external conditions.

From the above discussion it is clear that if the chip select setup time prior to the falling edge of the clock is met, the PI/T can consistently respond to a new read or write bus cycle every four clock cycles. This fact is especially useful in designing the PI/T's clock in synchronous bus systems not using $\overline{DTACK}$. (An extra clock period is required in interrupt acknowledge cycles, see **1.4.2 Interrupt Acknowledge Cycles**.)

In asynchronous bus systems in which the PI/T's clock differs from that of the bus master, generally there is no way to guarantee that the chip select setup time with respect to the PI/T clock is met. Thus, the only way to determine that the PI/T recognized the assertion of $\overline{CS}$ is to wait for the assertion of $\overline{DTACK}$. In this situation, all latched bus inputs to the PI/T must be held stable until $\overline{DTACK}$ is asserted. These include register select, R/$\overline{W}$, and write data inputs (see below).

System specifications impose a maximum delay from the trailing (negated) edge of $\overline{CS}$ to the negated edge of $\overline{DTACK}$. As system speeds increase this becomes more difficult to meet with a simple pullup resistor tied to the $\overline{DTACK}$ line. Therefore, the PI/T provides an internal active pullup device to reduce the rise time, and a level-sensitive circuit that later turns this device off. $\overline{DTACK}$ is negated asynchronously as fast as possible following the rising edge of chip select, then three-stated to avoid interference with the next bus cycle.

The system designer must take care that $\overline{DTACK}$ is negated and three-stated quickly enough after each bus cycle to avoid interference with the next one. With an M68000 this necessitates a relatively fast external path from the data strobe negation to $\overline{CS}$ bus master negation.

1.4.2 Interrupt Acknowledge Cycles

Special internal operations take place on PI/T interrupt acknowledge cycles. The port interrupt vector register or the timer vector register are implicitly addressed by the assertion of PC6/$\overline{PIACK}$ or PC7/$\overline{TIACK}$, respectively. The signals are first synchronized with the falling edge of the clock. One clock period after they are recognized, the data bus buffers are enabled and the vector is driven onto the bus. $\overline{DTACK}$ is asserted after another clock period to allow the vector some setup time prior to $\overline{DTACK}$. $\overline{DTACK}$ is negated, then three-stated, as with normal read or write cycles, when $\overline{PIACK}$ or $\overline{TIACK}$ is negated.

1.4.3 Write Cycles

In many ways, write cycles are similar to normal read cycles. On write cycles, data at the D0-D7 pins must meet the same setup specifications as the register select and R/$\overline{W}$ lines. Like these signals, write data is latched on the asserted edge of $\overline{CS}$, and must meet small setup and hold time requirements with respect to that edge. The same bus cycle recovery conditions exist as for normal read cycles. No other differences exist.

NOTE

For mask sets GG7 and KD1 if the RS lines are selecting the port interrupt vector register (PIVR) or timer interrupt vector register (TIVR) during an interrupt acknowledge bus cycle then those registers may be changed. Four cases exist for this situation, they are:

1. Case: RS lines are addressing PIVR during a port interrupt acknowledge cycle (PIACK asserted).
   Results: Incorrect IACK vector on data lines, bits 0 and 1 are zero, PIVR and TIVR remain the same and are not changed.
2. Case: RS lines are addressing TIVR during a port interrupt acknowledge cycle (PIACK asserted).
   Results: Incorrect IACK vector on data lines, PIVR and TIVR are changed.
3. Case: RS lines are addressing PIVR during a timer interrupt acknowledge cycle (TIACK asserted).
   Results: Incorrect IACK vector on data lines, PIVR and TIVR are changed.
4. Case: RS lines are addressing TIVR during a timer interrupt acknowledge cycle (TIACK asserted).
   Results: Correct IACK vector on data lines, PIVR and TIVR remain the same and are not changed.

For MC68000 and MC68010 systems that use A1-A5 for RS lines RS1-RS5 the above cases will never occur. A5 and A4 will remain high during interrupt acknowledge cycles and thus PIVR and TIVR will not be selected as shown below.

	RS5	RS4	RS3	RS2	RS1
			— Encoded Level —		
MC68000 IACK Cycle	1	1			
MC68230 PIVR Address	0	0	1	0	1
MC68230 TIVR Address	1	0	0	0	1

SECTION 2
PORT GENERAL INFORMATION AND CONVENTIONS

This section introduces concepts that are generally applicable to the PI/T ports independent of the chosen mode and submode. For this reason, no particular port or handshake pins are mentioned; the notation H1(H3) indicates that, depending on the chosen mode and submode, the statement given may be true for either the H1 or H3 handshake pin.

2.1 UNIDIRECTIONAL VS BIDIRECTIONAL

Figure 1-2 shows the configuration of ports A and B and each of the handshake pins in each port mode and submode. In modes 0 and 1, a data direction register is associated with each of the ports. These registers contain one bit for each port pin to determine whether that pin is an input or an output. Modes 0 and 1 are, thus, called unidirectional modes because each pin assumes a constant direction, changeable only by a reset condition or a programming change. These modes allow double-buffered data transfers in one direction. This direction, determined by the mode and submode definition, is known as the primary direction. Data transfers in the primary direction are controlled by the handshake pins. Data transfers not in the primary direction are generally unrelated, and single or unbuffered data paths exist.

In modes 2 and 3 there is no concept of primary direction as in modes 0 and 1. Except for port A in mode 2 (bit I/O), the data direction registers have no effect. These modes are bidirectional, in that the direction of each transfer (always 8 or 16 bits, double buffered) is determined dynamically by the state of the handshake pins. Thus, for example, data may be transferred out of the ports, followed very shortly by a transfer into the same port pins. Transfers to and from the ports are independent and may occur in any sequence. Since the instantaneous direction is always determined by the external system, a small amount of arbitration logic may be required.

2.1.1 Control of Double-Buffered Data Ports

Generally speaking, the PI/T is a double-buffered device. In the primary direction, double buffering allows orderly transfers by using the handshake pins in any of several programmable protocols. (When bit I/O is used, double buffering is not available and the handshake pins are used as outputs or status/interrupt inputs.)

Use of double buffering is most beneficial in situations where a peripheral device and the computer system are capable of transferring data at roughly the same speed. Double buffering allows the fetch operation of the data transmitter to be overlapped with the store operation of the data receiver. Thus, throughput measured in bytes or words-per-second may be greatly enhanced. If there is a large mismatch in transfer capability between the computer and the peripheral, little or no benefit is obtained. In these cases there is no penalty in using double buffering.

2.1.2 Double-Buffered Input Transfers

In all modes, the PI/T supports double-buffered input transfers. Data that meets the port setup and hold times is latched on the asserted edge of H1(H3). H1(H3) is edge sensitive, and may assume any duty cycle as long as both high and low minimum times are observed. The PI/T contains a port status register whose H1S(H3S) status bit is set anytime any input data that has not been read by the bus master is present in the double-buffered latches. The action of H2(H4) is programmable; it may indicate whether there is room for more data in the PI/T latches or it may serve other purposes. The following options are available, depending on the mode.

1. H2(H4) may be an edge-sensitive input that is independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by the direct method (refer to **2.3 DIRECT METHOD OF RESETTING STATUS**), the $\overline{\text{RESET}}$ pin being asserted, or when the H12 enable (H34 enable) bit of the port general control register is zero.
2. H2(H4) may be a general purpose output pin that is always negated. The H2S(H4S) status bit is always zero.
3. H2(H4) may be a general purpose output pin that is always asserted. The H2S(H4S) status bit is always zero.
4. H2(H4) may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H1(H3) input. As soon as the input latches become ready, H2(H4) is again asserted. When both double-buffered latches are full, H2(H4) remains negated until data is removed by a read of port A (port B) data register. Thus, anytime the H2(H4) output is asserted, new input data may be entered by asserting H1(H3). At other times transitions of H1(H3) are ignored. The H2S(H4S) status bit is always zero. When H12 enable (H34 enable) is zero, H2(H4) is held negated.

5. H2(H4) may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol, but never remains asserted longer than four clock cycles. Typically, a four clock cycle pulse is generated. But in the case that a subsequent H1(H3) asserted edge occurs before termination of the pulse, H2(H4) is negated asynchronously. Thus, anytime after the leading edge of the H2(H4) pulse, new data may be entered in the PI/T double-buffered input latches. The H2S(H4S) status bit is always zero. When H12 enable (H34 enable) is zero, H2(H4) is held negated.

A sample timing diagram is shown in Figure 2-1. The H2(H4) interlocked and pulse input handshake protocols are shown. The $\overline{\text{DMAREQ}}$ pin is also shown assuming it is enabled. All handshake pin sense bits are assumed to be zero (refer to **4.1 PORT GENERAL CONTROL REGISTER (PGCR)**); thus, the pins are in the low state when asserted. Due to the great similarity between modes, this timing diagram is applicable to all double-buffered input transfers.

2.1.3 Double-Buffered Output Transfers

The PI/T supports double-buffered output transfers in all modes. Data, written by the bus master to the PI/T, is stored in the port's output latch. The peripheral accepts the data by asserting H1(H3), which causes the next data to be moved to the port's output latch as soon as it is available. The function of H2(H4) is programmable; it may indicate whether new data has been moved to the output latch or it may serve other purposes. The H1S(H3S) status bit may be programmed for two interpretations. First, the status bit is a one when there is at least one latch in the double-buffered data path that can accept new data. After writing one byte/word of data to the ports, an interrupt

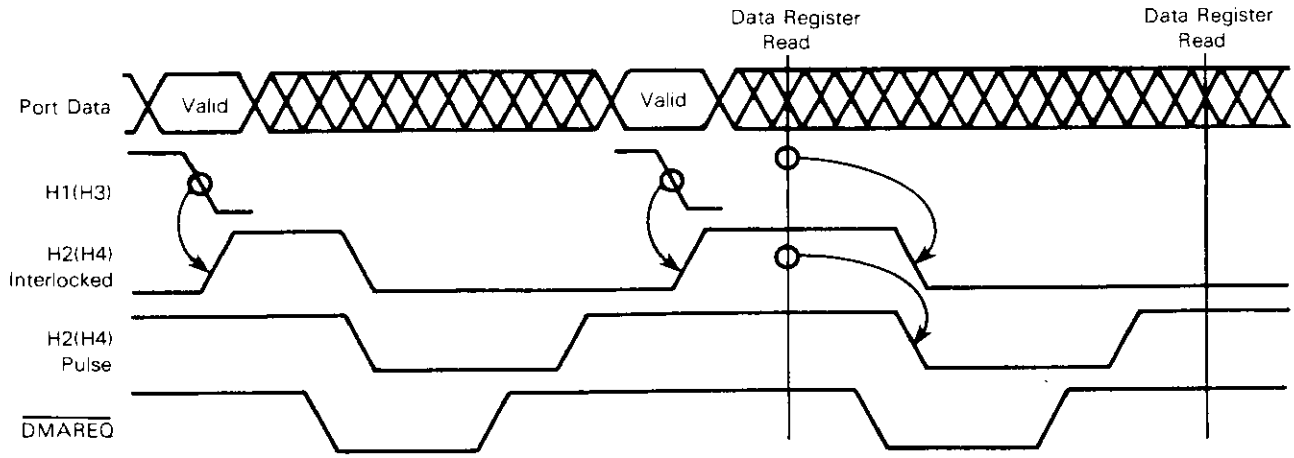


Figure 2-1. Double-Buffered Input Transfers Timing Diagram

service routine could check this bit to determine if it could store another byte/word, thus filling both latches. Second, when the bus master is finished, it is often useful to be able to check whether all of the data has been transferred to the peripheral. The H1S(H3S) status bit is set when both output latches are empty. The programmable options of the H2(H4) pin are given below, depending on the mode.

1. H2(H4) may be an edge-sensitive input pin independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by the direct method (refer to **2.3 DIRECT METHOD OF RESETTING STATUS**), the $\overline{\text{RESET}}$ pin being asserted, or when the H12 enable (H34 enable) bit of the port general control register is zero.
2. H2(H4) may be a general-purpose output pin that is always negated. The H2S(H4S) status bit is always zero.
3. H2(H4) may be a general-purpose output pin that is always asserted. The H2S(H4S) status bit is always zero.
4. H2(H4) may be an output pin in the interlocked output handshake protocol. H2(H4) is asserted two clock cycles after data is transferred to the double-buffered output latches. The data remains stable and H2(H4) remains asserted until the next asserted edge of the H1(H3) input. At that time, H2(H4) is asynchronously negated. As soon as the next data is available, it is transferred to the output latches and H2(H4) is asserted. When H2(H4) is negated, asserted transitions on H1(H3) have no effect on the data paths. As is explained later, however, in modes 2 and 3 H1 does control the three-state output buffers of the bidirectional port(s). The H2S(H4S) status bit is always zero. When H12 enable (H34 enable) is zero, H2(H4) is held negated.
5. H2(H4) may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked output protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock pulse is generated. But in the case that a subsequent H1(H3) asserted edge occurs before termination of the pulse, H2(H4) is negated asynchronously, thus shortening the pulse. The H2S(H4S) status bit is always zero. When H12 enable (H34 enable) is zero, H2(H4) is held negated.

A sample timing diagram is shown in Figure 2-2. The H2(H4) interlocked and pulsed output handshake protocols are shown. The $\overline{\text{DMAREQ}}$ pin is also shown assuming it is enabled. All handshake pin sense bits are assumed to be zero; thus, the pins are in the low state when asserted. Due to the great similarity between modes, this timing diagram is applicable to all double-buffered output transfers.

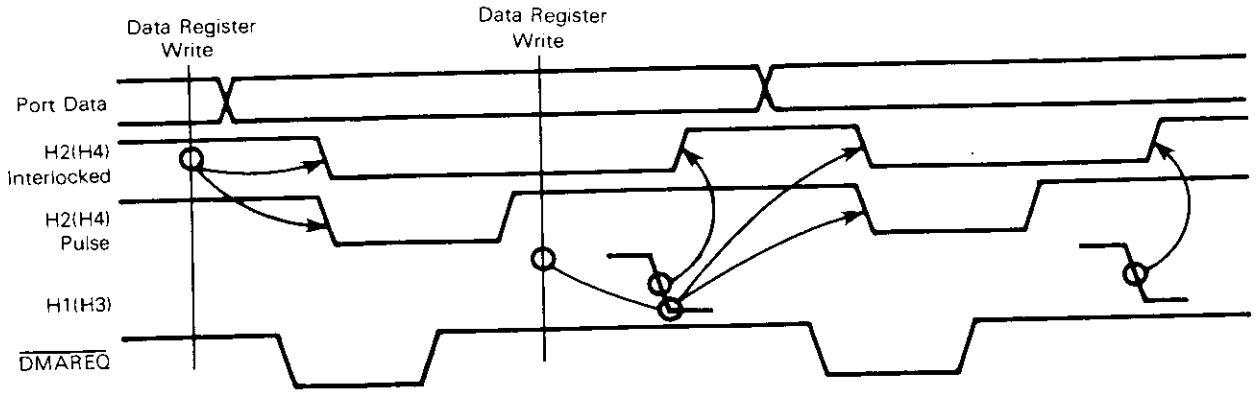


Figure 2-2. Double-Buffered Output Transfers Timing Diagram

2.2 REQUESTING BUS MASTER SERVICE

The PI/T has several means of indicating a need for service by a bus master. First, the processor may poll the port status register. It contains a status bit for each handshake pin, plus a level bit that always reflects the instantaneous state of that handshake pin. A status bit is one when the PI/T needs servicing (i.e., generally when the bus master needs to read or write data to the ports) or when a handshake pin used as a simple status input has been asserted. The interpretation of these bits is dependent on the chosen mode and submode.

Second, the PI/T may be placed in the processor's interrupt structure. As mentioned previously, the PI/T contains port A and B control registers that configure the handshake pins. Other bits in these registers enable an interrupt associated with each handshake pin. This interrupt is made available through the PC5/$\overline{\text{PIRQ}}$ pin, if the $\overline{\text{PIRQ}}$ function is selected. Three additional conditions are required for $\overline{\text{PIRQ}}$ to be asserted: 1) the handshake pin status bit is set, 2) the corresponding interrupt (service request) enable bit is set, and 3) DMA requests are not associated with that data transfer (H1 and H3 only). The conditions from each of the four handshake status bits and corresponding status bits are ORed to determine $\overline{\text{PIRQ}}$. To clear the interrupt, the proper status bit must be cleared (see **2.3 DIRECT METHOD OF RESETTING STATUS**).

The third method of requesting service is via the PC4/$\overline{\text{DMAREQ}}$ pin. This pin can be associated with double-buffered transfers in each mode. If it is used as a DMA controller request, it can initiate requests to keep the PI/T's input/output double-buffering empty/full as much as possible. It will not overrun the DMA controller. The pin is compatible with the MC68450 direct memory access controller (DMAC).

2.2.1 Vectored, Prioritized Port Interrupts

Use of MC68000-compatible vectored interrupts with the PI/T requires the $\overline{\text{PIRQ}}$ and $\overline{\text{PIACK}}$ pins. When $\overline{\text{PIACK}}$ is asserted while $\overline{\text{PIRQ}}$ is asserted, the PI/T places an 8-bit vector on the data pins D0-D7. Under normal conditions, this vector corresponds to the highest priority enabled active port interrupt source with which the $\overline{\text{DMAREQ}}$ pin is not currently associated. The most-significant six bits are provided by the port interrupt vector register (PIVR), with the lower two bits supplied by prioritization logic according to conditions present when $\overline{\text{PIACK}}$ is asserted. It is important to note that the only effect on the PI/T caused by interrupt acknowledge cycles is that the vector is placed on the data bus. Specifically, no registers, data, status, or other internal states of the PI/T are affected by the cycle.

Several conditions may be present when the $\overline{\text{PIACK}}$ input is asserted to the PI/T. These conditions affect the PI/T's response and the termination of the bus cycle. If the PI/T has no interrupt function selected, or is not asserting $\overline{\text{PIRQ}}$, the PI/T will make no response to $\overline{\text{PIACK}}$ ($\overline{\text{DTACK}}$ will not be asserted). If the PI/T is asserting $\overline{\text{PIRQ}}$ when $\overline{\text{PIACK}}$ is received, the PI/T will output the contents of the port interrupt vector register and the prioritization bits. If the PIVR has not been initialized, $0F will be read from this register. These conditions are summarized in Table 2-1.

Table 2-1. Response to Port Interrupt Acknowledge

Conditions	$\overline{\text{PIRQ}}$ negated OR interrupt request function not selected	$\overline{\text{PIRQ}}$ asserted
PIVR has not been initialized since $\overline{\text{RESET}}$	No response from PI/T. No $\overline{\text{DTACK}}$.	PI/T provides $0F, the Uninitialized Vector*
PIVR has been initialized since $\overline{\text{RESET}}$	No response from PI/T. No $\overline{\text{DTACK}}$.	PI/T provides PIVR contents with prioritization bits.

* The uninitialized vector is the value returned from an interrupt vector register before it has been initialized.

The vector table entries for the PI/T appear as a contiguous block of four vector numbers whose common upper six bits are programmed in the PIVR. The following table pairs each interrupt source with the 2-bit value provided by the prioritization logic when interrupt acknowledge is asserted (see **4.2. PORT SERVICE REQUEST REGISTER (PSRR)**).

H1 source — 00
H2 source — 01
H3 source — 10
H4 source — 11

2.2.2 Autovectored Port Interrupts

Autovectored interrupts use only the $\overline{\text{PIRQ}}$ pin. The operation of the PI/T with vectored and autovectored interrupts is identical except that no vectors are supplied and the PC6/$\overline{\text{PIACK}}$ pin can be used as a port C pin.

2.2.3 DMA Request Operation

The direct memory access request ($\overline{\text{DMAREQ}}$) pulse (when enabled) is associated with output or input transfers to keep the initial and final output latches full or initial and final input latches empty, respectively. Figures 2-3 and 2-4 show all the possible paths in generating DMA requests. See **4.2 PORT SERVICE REQUEST REGISTER (PSRR)** for programming the operation of the DMA request bit.

$\overline{\text{DMAREQ}}$ is generated on the bus side of the MC68230 by the synchronized* chip select. If the conditions of Figures 2-3 or 2-4 are met, an assertion of $\overline{\text{CS}}$ will cause $\overline{\text{DMAREQ}}$ to be asserted three PI/T clocks (plus the delay time from the clock edge) after $\overline{\text{CS}}$ is synchronized. $\overline{\text{DMAREQ}}$ remains asserted three clock cycles (plus the delay time from the clock edge) and is then negated.

$\overline{\text{DMAREQ}}$ pulses are associated with peripheral transfers or are generated by the synchronized* H1(H3) input. If the conditions of Figures 2-3 or 2-4 are met, an assertion of the H1(H3) input will cause $\overline{\text{DMAREQ}}$ to be asserted 2.5 PI/T clock cycles (plus the delay time from clock edge) after H1(H3) is synchronized. $\overline{\text{DMAREQ}}$ remains asserted three clock cycles (plus the delay time from the clock edge) and is then negated.

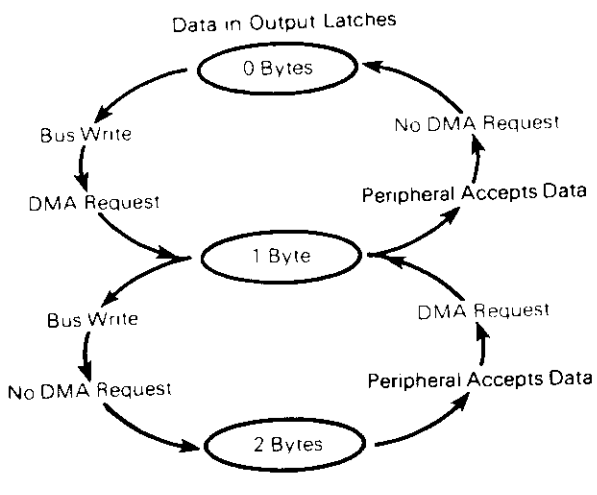


Figure 2-3. $\overline{\text{DMAREQ}}$ Associated with Output Transfers

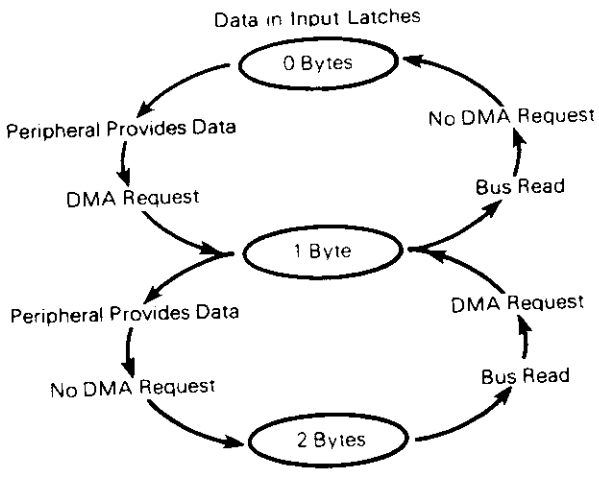


Figure 2-4. $\overline{\text{DMAREQ}}$ Associated with Input Transfers

2.3 DIRECT METHOD OF RESETTING STATUS

In certain modes one or more handshake pins can be used as edge-sensitive inputs for the sole purpose of setting bits in the port status register. These bits consist of simple flip-flops. They are set (to one) by the occurrence of the asserted edge of the handshake pin input. Resetting a handshake status bit can be done by writing an 8-bit mask to the port status register. This is called the direct method of resetting. To reset a status bit that is resettable by the direct method, the mask must

* Synchronized means that the appropriate input signal (H1, H3, or $\overline{\text{CS}}$) has been sampled by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for $\overline{\text{CS}}$). Refer to **1.4 BUS INTERFACE OPERATION** for the exception concerning $\overline{\text{CS}}$. If a bus access (assertion of $\overline{\text{CS}}$) and a port access (assertion of H1(H3)) occur at the same time, $\overline{\text{CS}}$ will be recognized without any delay. H1(H3) will be recognized one clock cycle later.

contain a one in the bit position of the port status register corresponding to the desired status bit. For status bits that are not resettable by the direct method in the chosen mode, the data written to the port status register has no effect. For status bits that are resettable by the direct method in the chosen mode, a zero in the mask has no effect.

2.4 HANDSHAKE PIN SENSE CONTROL

The PI/T contains exclusive-OR gates to control the sense of each of the handshake pins, whether used as inputs or outputs. Four bits in the port general control register may be programmed to determine whether the pins are asserted in the low- or high-voltage state. As with other control registers, these bits are reset to zero when the $\overline{\text{RESET}}$ pin is asserted, defaulting the asserted level to be low.

2.5 ENABLING PORTS A AND B

Certain functions involved with double-buffered data transfers, the handshake pins, and the status bits may be disabled by the external system or by the programmer during initialization. The port general control register contains two bits, H12 enable and H34 enable, which control these functions. These bits are cleared to the zero state when the $\overline{\text{RESET}}$ pin is asserted, and the functions are disabled. The functions are the following:

1. Independent of other actions by the bus master or peripheral (via the handshake pins), the PI/T's disabled handshake controller is held to the "empty" state; i.e., no data is present in the double-buffered data path.
2. When any handshake pin is used to set a simple status flip-flop, unrelated to double-buffered transfers, these flip-flops are held reset to zero (see Table 1-1).
3. When H2(H4) is used in an interlocked or pulsed handshake with H1(H3), H2(H4) is held negated, regardless of the chosen mode, submode, and primary direction. Thus, for double-buffered input transfers, the programmer may signal a peripheral when the PI/T is ready to begin transfers by setting the associated handshake enable bit to one.

2.6 PORT A AND B ALTERNATE REGISTERS

In addition to the port A and B data registers, the PI/T contains port A and B alternate registers. These registers are read only, and simply provide the instantaneous (non-latched) level of each port pin. They have no effect on the operation of the handshake pins, double-buffered transfers, status bits, or any other aspect of the PI/T, and they are mode/submode independent. Refer to **4.7 PORT ALTERNATE REGISTERS** for further information.

SECTION 3
PORT MODES

This section contains information that distinguishes the various port modes and submodes. General characteristics common to all modes are defined in **SECTION 2 PORT GENERAL INFORMATION AND CONVENTIONS.** A description of the port A control register (PACR) and port B control register (PBCR) is given before each mode description. After each submode description, the programmable options are listed for that submode.

3.1 PORT A CONTROL REGISTER

Port A Control Register (PACR)

7	6	5	4	3	2	1	0
Port A Submode		H2 Control			H2 Interrupt Enable	H1 SVCRQ Enable	H1 Status Control

The port A control register, in conjunction with the programmed mode and the port B submode, controls the operation of port A and the handshake pins H1 and H2. The port A control register contains five fields: bits 7 and 6 specify the port A submode; bits 5, 4, and 3 control the operation of the H2 handshake pin and the H2S status bit; bit 2 determines whether an interrupt will be generated when the H2S status bit goes to one; and bit 1 determines whether a service request (interrupt request or DMA request) will occur; bit 0 controls the operation of the H1S status bit. The PACR is always readable and writable.

All bits are cleared to zero when the $\overline{\text{RESET}}$ pin is asserted. When the port A submode field is relevant in a mode/submode definition, it must not be altered unless the H12 enable bit in the port general control register is clear (see Table 1-3 located on foldout pages 1 and 2 at the end of this document). Altering these bits will give unpredictable results.

3.2 PORT B CONTROL REGISTER

Port B Control Register (PBCR)

7	6	5	4	3	2	1	0
Port B Submode		H4 Control			H4 Interrupt Enable	H3 SVCRQ Enable	H3 Status Control

The port B control register specifies the operation of port B and the handshake pins H3 and H4. The port B control register contains five fields: bits 7 and 6 specify the port B submode; bits 5, 4, and 3 control the operation of the H4 handshake pin and H4S status bit; bit 2 determines whether an interrupt will be generated when the H4S status bit goes to a one; bit 1 determines whether a service request (interrupt request or DMA request) will occur; and bit 0 controls the operation of the H3S status bit. The PBCR is always readable and writable. There is never a consequence to reading the register.

All bits are cleared to zero when the $\overline{\text{RESET}}$ pin is asserted. When the port B submode field is relevant in a mode/submode definition, it must not be altered unless the H34 enable bit in the port general control register is clear (see Table 1-3 located on foldout pages 1 and 2 at the end of this document).

3.3 MODE 0 — UNIDIRECTIONAL 8-BIT MODE

In mode 0, ports A and B operate independently. Each may be configured in any of its three possible submodes:

Submode 00 — Pin-Definable Double-Buffered Input or Single-Buffered Output
Submode 01 — Pin-Definable Double-Buffered Output or Non-Latched Input
Submode 1X — Bit I/O (Pin-Definable Single-Buffered Output or Non-Latched Input)

Handshake pins H1 and H2 are associated with port A and configured by programming the port A control register. (The H12 enable bit of the port general control register enables port A transfers.) Handshake pins H3 and H4 are associated with port B and configured by programming the port B control register. (The H34 enable bit of the port general control register enables port B transfers.) The port A and B data direction registers operate in all three submodes. Along with the submode, they affect the data read and write at the associated data register according to Table 3-1. They also enable the output buffer associated with each port pin. The $\overline{\text{DMAREQ}}$ pin may be associated with either (not both) port A or port B, but does not function if the bit I/O submode (submode 1X) is programmed for the chosen port.

Table 3-1. Mode 0 Port Data Paths

Mode	Read Port A/B Data Register		Write Port A/B Data Register	
	DDR = 0	DDR = 1	DDR = X	
0 Submode 00	FIL, D.B.	FOL Note 3	FOL, S.B.	Note 1
0 Submode 01	Pin	FOL Note 3	IOL/FOL, D.B.	Note 2
0 Submode 1X	Pin	FOL Note 3	FOL, S.B.	Note 1

Abbreviations:
IOL — Initial Output Latch
FOL — Final Output Latch
FIL — Final Input Latch
S.B. — Single Buffered
D.B. — Double Buffered
DDR — Data Direction Register

Note 1: Data is latched in the output data registers (final output latch) and will be single buffered at the pin if the DDR is 1. The output buffers will be turned off if the DDR is 0.
Note 2: Data is latched in the double-buffered output data registers. The data in the final output latch will appear on the port pin if the DDR is a 1.
Note 3: The output drivers that connect the final output latch to the pins are turned on.

3.3.1 Submode 00 — Pin-Definable Double-Buffered Input or Single-Buffered Output

In mode 0, double-buffered input transfers of up to eight bits are available by programming submode 00 in the desired port's control register. Data that meets the port setup and hold times is latched on the asserted edge of H1(H3) and is placed in the initial or final input latch. H1(H3) is edge sensitive and may assume any duty cycle as long as both high and low minimum times are observed. The PI/T contains a port status register whose H1S(H3S) status bit is set anytime any input data that has not been read by the bus master is present in the double-buffered latches. The action of H2(H4) is programmable. The following options are available:

1. H2(H4) may be an edge-sensitive status input that is independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status register (PSR), or when the H12 enable (H34 enable) bit of the port general register is clear.
2. H2(H4) may be a general-purpose output pin that is always negated. In this case the H2S(H4S) status bit is always clear.
3. H2(H4) may be a general-purpose output pin that is always asserted. In this case the H2S(H4S) status bit is always clear.
4. H2(H4) may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H1(H3) input. As soon as the input latches become ready, H2(H4) is again asserted. When the input double-buffered latches are full, H2(H4) remains negated until data is removed. Thus, anytime the H2(H4) output is asserted, new input data may be entered by asserting H1(H3). At other times, transitions on H1(H3) are ignored. The H2S(H4S) status bit is always clear. When H12 enable (H34 enable) in the port general control register is clear, H2(H4) is held negated.
5. H2(H4) may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock cycle pulse is generated. But in the case of a subsequent H1(H3) asserted edge occurring before termination of the pulse, H2(H4) is negated asynchronously. Thus, anytime after the leading edge of the H2(H4) pulse, new data may be entered in the double-buffered input latches. The H2S(H4S) status bit is always clear. When H12 enable (H34 enable) is clear, H2(H4) is held negated.

For pins used as outputs, the data path consists of a single latch driving the output buffer. Data written to the port's data register does not affect the operation of any handshake pin or status bit. Output pins may be used independently of the input transfers. However, read bus cycles to the data register do remove data from the port. Therefore, care should be taken to avoid processor instructions that perform unwanted read cycles.

Programmable Options Mode 0 — Port A Submode 00 and Port B Submode 00 (Sheet 1 of 2)

PACR 7 6	Port A Submode
0 0	Submode 00

PACR 5 4 3	H2 Control
0 X X	Input pin — edge-sensitive status input, H2S is set on an asserted edge.
1 0 0	Output pin — negated, H2S is always clear.
1 0 1	Output pin — asserted, H2S is always clear.
1 1 0	Output pin — interlocked input handshake protocol, H2S is always clear.
1 1 1	Output pin — pulsed input handshake protocol, H2S is always clear.

PACR 2	H2 Interrupt Enable
0	The H2 interrupt is disabled.
1	The H2 interrupt is enabled.

Programmable Options Mode 0 — Port A Submode 00 and Port B Submode 00 (Sheet 2 of 2)

PACR
1 — **H1 SVCR Enable**

0	The H1 interrupt and DMA request are disabled.
1	The H1 interrupt and DMA request are enabled.

PACR
0 — **H1 Status Control**

X	The H1S status bit is set anytime input data is present in the double-buffered input path.

PBCR
7 6 — **Port B Submode**

0 0	Submode 00

PBCR
5 4 3 — **H4 Control**

0 X X	Input pin — edge-sensitive status input, H4S is set on an asserted edge.
1 0 0	Output pin — negated, H4S is always cleared.
1 0 1	Output pin — asserted, H4S is always cleared.
1 1 0	Output pin — interlocked input handshake protocol, H4S is always cleared.
1 1 1	Output pin — pulsed input handshake protocol, H4S is always cleared.

PBCR
2 — **H4 Interrupt Enable**

0	The H4 interrupt is disabled.
1	The H4 interrupt is enabled.

PBCR
1 — **H3 SVCRQ Enable**

0	The H3 interrupt and DMA request are disabled.
1	The H3 interrupt and DMA request are enabled.

PBCR
0 — **H3 Status Control**

X	The H3S status bit is set anytime input data is present in the double-buffered input path.

3.3.2 Submode 01 — Pin-Definable Double-Buffered Output or Non-Latched Input

In mode 0, double-buffered output transfers of up to eight bits are available by programming submode 01 in the desired port's control register. The operation of H2 and H4 may be selected by programming the port A and B control registers, respectively. Data, written by the bus master to the PI/T, is stored in the port's output latches. The peripheral accepts the data by asserting H1(H3), which causes the next data to be moved to the port's output latch as soon as it is available.

The H1S(H3S) status bit may be programmed for two interpretations:

1. The H1S(H3S) status bit is set when either the port initial or final output latch can accept new data. It is cleared when both latches are full and cannot accept new data.
2. The H1S(H3S) status bit is set when both of the port output latches are empty. It is cleared when at least one latch is full.

The programmable options of the H2(H4) pin are:

1. H2(H4) may be an edge-sensitive input pin independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by either the

$\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status register (PSR), or when the H1(H2) enable (H3(H4) enable) bit of the port general control register is clear.

2. H2(H4) may be a general-purpose output pin that is always negated. The H2S(H4S) status bit is always clear.
3. H2(H4) may be a general-purpose output pin that is always asserted. The H2S(H4S) status bit is always clear.
4. H2(H4) may be an output pin in the interlocked output handshake protocol. H2(H4) is asserted two clock cycles after data is transferred to the double-buffered output latches. The data remains stable at the port pins and H2(H4) remains asserted until the next asserted edge of the H1(H3) input. At that time, H2(H4) is asynchronously negated. As soon as the next data is available, it is transferred to the output latches. When H2(H4) is negated, asserted transitions of H1(H3) have no affect on data paths. The H2S(H4S) status bit is always clear. When H12 enable (H34 enable) is clear, H2(H4) is held negated.
5. H2(H4) may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock pulse is generated. But in the case that a subsequent H1(H3) asserted edge occurs before termination of the pulse, H2(H4) is negated asynchronously shortening the pulse. The H3S(H4S) status bit is always clear. When H12 enable (H34 enable) is clear H2(H4) is held negated.

For pins used as inputs, data written to the associated data register is double-buffered and passed to the initial or final output latch, but, the output buffer is disabled.

Programmable Options Mode 0 — Port A Submode 01 and Port B Submode 01 (Sheet 1 of 2)

PACR 7 6	Port A Submode
0 1	Submode 01

PACR 5 4 3	H2 Control
0 X X	Input pin — edge-sensitive status input, H2S is set on an asserted edge.
1 0 0	Output pin — negated, H2S is always clear.
1 0 1	Output pin — asserted, H2S is always clear.
1 1 0	Output pin — interlocked input handshake protocol, H2S is always clear.
1 1 1	Output pin — pulsed input handshake protocol, H2S is always clear.

PACR 2	H2 Interrupt Enable
0	The H2 interrupt is disabled.
1	The H2 interrupt is enabled.

PACR 1	H1 SVCRQ Enable
0	The H1 interrupt and DMA request are disabled.
1	The H1 interrupt and DMA request are enabled.

Programmable Options Mode 0 — Port A Submode 01 and Port B Submode 01 (Sheet 2 of 2)

PACR
0 — **H1 Status Control**

0 The H1S status bit is set when either the port A initial or final output latch can accept new data. It is clear when both latches are full and cannot accept new data.

1 The H1S status bit is one when both of the port A output latches are empty. It is clear when at least one latch is full.

PBCR
7 6 — **Port B Submode**

0 1 Submode 01

PBCR
5 4 3 — **H4 Control**

0 X X Input pin — edge-sensitive status input, H4S is set on an asserted edge.
1 0 0 Output pin — negated, H4S is always cleared.
1 0 1 Output pin — asserted, H4S is always cleared.
1 1 0 Output pin — interlocked input handshake protocol, H4S is always cleared.
1 1 1 Output pin — pulsed input handshake protocol, H4S is always cleared.

PBCR
2 — **H4 Interrupt Enable**

0 The H4 interrupt is disabled.
1 The H4 interrupt is enabled.

PBCR
1 — **H3 SVCRQ Enable**

0 The H3 interrupt and DMA request are disabled.
1 The H3 interrupt and DMA request are enabled.

PBCR
0 — **H3 Status Control**

0 The H3S status bit is set when either the port B initial or final output latch can accept new data. It is clear when both latches are full and cannot accept new data.

1 The H3S status bit is one when both of the port B output latches are empty. It is clear when at least one latch is full.

3.3.3 Submode 1X — Bit I/O (Pin-Definable Single-Buffered Output or Non-Latched Input)

In mode 0, simple bit I/O is available by programming submode 1X in the desired port's control register. This submode is intended for applications in which several independent devices must be controlled or monitored. Data written to the associated (input/output) register is single buffered. If the data direction register bit for that pin is a one (output), the output buffer is enabled. If it is a zero (input), data written is still latched, but is not available at the pin. Data read from the data register is the instantaneous value of the pin or what was written to the data register, depending on the contents of the data direction register. H1(H3) is an edge-sensitive status input pin only and it controls no data related function. The H1S(H3S) status bit is set following the asserted edge of the input waveform. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the associated status bit in the port status register (PSR), or when the H12 enable (H34 enable) bit of the port general control register is clear. H2 may be programmed as:

1. H2(H4) may be an edge-sensitive status input that is independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status

register (PSR), or when the H12 enable (H34 enable) bit of the port general control register is clear.

2. H2(H4) may be a general-purpose output pin that is always negated. In this case the H2S(H4S) status bit is always clear.
3. H2(H4) may be a general-purpose output pin that is always asserted. In this case the H2S(H4S) status bit is always clear.

Programmable Option Mode 0 — Port A Submode 1X and Port B Submode 1X (Sheet 1 of 2)

PACR 7 6	Port A Submode
1 X	Submode 1X

PACR 5 4 3	H2 Control
0 X X	Input pin — edge-sensitive status input, H2S is set on an asserted edge.
1 X 0	Output pin — negated, H2S is always cleared.
1 X 1	Output pin — asserted, H2S is always cleared.

PACR 2	H2 Interrupt Enable
0	The H2 interrupt is disabled.
1	The H2 interrupt is enabled.

PACR 1	H1 SVCRQ Enable
0	The H1 interrupt is disabled.
1	The H1 interrupt is enabled.

PACR 0	H1 Status Control
X	H1 is an edge-sensitive status input, H1S is set by an asserted edge of H1.

PBCR 7 6	Port B Submode
1 X	Submode 1X

PBCR 5 4 3	H4 Control
0 X X	Input pin — edge-sensitive status input, H4S is set on an asserted edge.
1 X 0	Output pin — negated, H4S is always cleared.
1 X 1	Output pin — asserted, H4S is always cleared.

PBCR 2	H4 Interrupt Enable
0	The H4 interrupt is disabled.
1	The H4 interrupt is enabled.

PBCR 1	H3 SVCRQ Enable
0	The H3 interrupt is disabled.
1	The H3 interrupt is enabled.

Programmable Options Mode 0 — Port A Submode 1X and Port B Submode 1X (Sheet 2 of 2)

PBCR	
0	**H3 Status Control**
X	H3 is an edge-sensitive status input, H3S is set by an asserted edge of H3.

3.4 MODE 1 — UNIDIRECTIONAL 16-BIT MODE

In mode 1, ports A and B are concatenated to form a single 16-bit port. The port B submode field controls the configuration of both ports. The possible submodes are:

Port B Submode X0 — Pin-Definable Double-Buffered Input or Single-Buffered Output

Port B Submode X1 — Pin-Definable Double-Buffered Output or Non-Latched Input

Handshake pins H3 and H4, configured by programming the port B control register, are associated with the 16-bit double-buffered transfer. These 16-bit transfers are enabled by setting the H34 enable bit in the port general control register (PGCR). Handshake pins H1 and H2 may be used as simple status inputs not related to the 16-bit data transfer or H2 may be an output. Enabling of the H1 and H2 handshake pins is done by setting the H12 enable bit of the port general control register. The port A and B data direction registers operate in each submode. Along with the submode, they affect the data read and written at the data register according to Table 3-2. The data direction register also enables the output buffer associated with each port pin. The $\overline{\text{DMAREQ}}$ pin may be associated only with H3.

Table 3-2. Mode 1 Port Data Paths

Mode	Read Port A/B Register		Write Port A/B Register	
	DDR = 0	DDR = 1	DDR = 0	DDR = 1
1, Port B Submode X0	FIL, D.B.	FOL Note 3	FOL, S.B. Note 2	FOL, S.B. Note 2
1, Port B Submode X1	Pin	FOL Note 3	IOL/FOL, D.B., Note 1	IOL/FOL, D.B., Note 1

Note 1: Data written to Port A goes to a temporary latch. When the Port B data register is later written, Port A data is transferred to IOL/FOL.
Note 2: Data is latched in the output data registers (final output latch) and will be single buffered at the pin if the DDR is 1. The output buffers will be turned off if the DDR is 0.
Note 3: The output drivers that connect the final output latch to the pins are turned on.

Abbreviations:
IOL — Initial Output Latch
FOL — Final Output Latch
FIL — Final Input Latch
S.B. — Single Buffered
D.B. — Double Buffered
DDR — Data Direction Register

Mode 1 can provide convenient high-speed 16-bit transfers. The port A and port B data registers are addressed for compatibility with the MC68000 move peripheral (MOVEP) instruction and with the MC68450 direct memory access controller (DMAC). To take advantage of this, port A should contain the most-significant byte of data and always be read or written by the bus master first. The interlocked and pulsed handshake protocols, status bits, and $\overline{\text{DMAREQ}}$ are keyed to the access of port B data register in mode 1. Transfers proceed properly with interlocked or pulsed handshakes when the port B data register is accessed last.

3.4.1 Port A Control Register

Port A Control Register (PACR)

7	6	5	4	3	2	1	0
Port A Submode		H2 Control			H2 Interrupt Enable	H1 SVCRQ Enable	H1 Status Control

The port A control register, in conjunction with the programmed mode and the port B submode, controls the operation of port A and the handshake pins H1 and H2. The port A control register contains five fields: bits 7 and 6 specify the port A submode; bits 5, 4, and 3 control the operation of the H2 handshake pin and H2S status bit; bit 2 determines whether an interrupt will be generated when the H2S status bit goes to one; bit 1 determines whether a service request (interrupt request or DMA request) will occur; and bit 0 controls the operation of the H1S status bit. The PACR is always readable and writable. There is never a consequence to reading the register.

All bits are cleared to zero when the $\overline{\text{RESET}}$ pin is asserted. When the port A submode field is relevant in a mode/submode definition, it must not be altered unless the H12 enable bit in the port general control register is clear (see Table 1-3 located on foldout pages 1 and 2 at the end of this document). Altering these bits may give unpredictable results if the H12 enable bit in the PGCR is set.

3.4.2 Port B Control Register

Port B Control Register (PBCR)

7	6	5	4	3	2	1	0
Port B Submode		H4 Control			H4 Interrupt Enable	H3 SVCRQ Enable	H3 Status Control

The port B control register specifies the operation of port B and the handshake pins H3 and H4. The port B control register contains five fields: bits 7 and 6 specify the port B submode; bits 5, 4, and 3 control the operation of the H4 handshake pin and H4S status bit goes to a one; bit 1 determines whether a service request (interrupt request or DMA request) will occur; and bit 0 controls the operation of the H3S status bit. The PBCR is always readable and writable.

All bits are cleared to zero when the $\overline{\text{RESET}}$ pin is asserted. When the port B submode field is relevant in a mode/submode definition, it must not be altered unless the H34 enable bit in the port general control register is clear (see Table 1-3 located on foldout pages 1 and 2 at the end of this document). Altering these bits may give unpredictable results if the H12 enable bit in the PGCR is set.

3.4.3 Submode X0 — Pin-Definable Double-Buffered Input or Single-Buffered Output

In mode 1 submode X0, double-buffered input transfers of up to 16 bits may be obtained. The level of each pin is asynchronously latched with the asserted edge of H3 and placed in the initial input latch or the final input latch. The processor may check the H3S status bit to determine if new data is present. The $\overline{\text{DMAREQ}}$ pin may be used to signal a DMA controller to empty the input buffers. Regardless of the bus master, port A data should be read first and port B data should be read last. The operation of the internal handshake controller, the H3S bit, and the $\overline{\text{DMAREQ}}$ are keyed to the reading of the port B data register. (The MC68450 DMAC can be programmed to perform the exact transfers needed for compatibility with the PI/T.) H4 may be programmed as:

1. H4 may be an edge-sensitive status input that is independent of H3 and the transfer of port data. On the asserted edge of H4, the H4S status bit is set. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status register (PSR), or when the H34 enable bit of the port general control register is clear.
2. H4 may be a general-purpose output pin that is always negated. In this case the H4S status bit is always clear.
3. H4 may be a general-purpose output pin that is always asserted. In this case the H4S status bit is always clear.
4. H4 may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H3 input. As soon as the input latches become ready, H4 is again asserted. When the input double-buffered latches are full, H4 remains negated until data is removed. Thus, anytime the H4 output is asserted, new input data may be entered by asserting H3. At other times transitions on H3 are ignored. The H4S status bit is always clear. When H34 enable in the port general control register is clear, H4 is held negated.
5. H4 may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock cycle pulse is generated. But in the case that a subsequent H3 asserted edge occurs before termination of the pulse, H4 is negated asynchronously. Thus, anytime after the leading edge of the H4 pulse, new data may be entered in the double-buffered input latches. The H4S status bit is always clear. When H34 enable is clear, H4 is held negated.

For pins used as outputs, the data path consists of a single latch driving the output buffer. Data written to the port's data register does not affect the operation of any handshake pin, status bit, or any other aspect of the PI/T. Thus, output pins may be used independently of the input transfer.

The programmable options of the H2 pin are:

1. H2 may be an edge-sensitive input pin independent of H1 and the transfer of port data. On the asserted edge of H2, the H2S status bit is set. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status register (PSR), or when the H12 enable bit of the port general control register is clear.
2. H2 may be a general-purpose output pin that is always negated. The H2S status bit is always clear.
3. H2 may be a general-purpose output pin that is always asserted. The H2S status bit is always clear.

Programmable Options Mode 1 — Port A Submode XX and Port B Submode X0

PACR
7 6 — Port A Submode
0 0 Submode XX

PACR
5 4 3 — H2 Control
0 X X Input pin — edge-sensitive status input, H2S is set on an asserted edge.
1 X 0 Output pin — negated, H2S is always cleared.
1 X 1 Output pin — asserted, H2S is always cleared.

PACR
2 — H2 Interrupt Enable
0 The H2 interrupt is disabled.
1 The H2 interrupt is enabled.

PACR
1 — H1 SVCRQ Enable
0 The H1 interrupt is disabled.
1 The H1 interrupt is enabled.

PACR
0 — H1 Status Control
X H1 is an edge-sensitive status input. H1S is set by an asserted edge of H1.

PBCR
7 6 — Port B Submode
0 0 Submode X0

PBCR
5 4 3 — H4 Control
0 X X Input pin — edge-sensitive status input, H4S is set on an asserted edge.
1 0 0 Output pin — negated, H4S is always cleared.
1 0 1 Output pin — asserted, H4S is always cleared.
1 1 0 Output pin — interlocked input handshake protocol.
1 1 1 Output pin — pulsed input handshake protocol.

PBCR
2 — H2 Interrupt Enable
0 The H4 interrupt is disabled.
1 The H4 interrupt is enabled.

PBCR
1 — H3 SVCRQ Enable
0 The H3 interrupt and DMA request are disabled.
1 The H3 interrupt and DMA request are enabled.

PBCR
0 — H3 Status Control
X The H3S status bit is set anytime input data is present in the double-buffered input path.

3.4.4 Submode X1 — Pin-Definable Double-Buffered Output or Non-Latched Input

In mode 1 submode X1, double-buffered output transfers of up to 16 bits may be obtained. Data is written by the bus master (processor or DMA controller) in two bytes. The first byte (most significant) is written to the port A data register. It is stored in a temporary latch until the next byte is written to the port B data register. Then all 16 bits are transferred to one of the output latches of ports A and B. The $\overline{\text{DMAREQ}}$ pin may be used to signal a DMA controller to transfer another word to the port output latches. (The MC68450 DMAC can be programmed to perform the exact transfers needed for compatibility with the PI/T.) H4 may be programmed as:

1. H4 may be an edge-sensitive status input that is independent of H3 and the transfer of port data. On the asserted edge of H4, the H4S status bit is set. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status register (PSR), or when the H34 enable bit of the port general control register is clear.
2. H4 may be a general-purpose output pin that is always negated. In this case the H4S status bit is always clear.
3. H4 may be a general-purpose output pin that is always asserted. In this case the H4S status bit is always clear.
4. H4 may be an output pin in the interlocked output handshake protocol. H4 is asserted two clock cycles after data is transferred to the double-buffered output latches. The data remains stable at the port pins and H4 remains asserted until the next asserted edge of the H3 input. At that time, H4 is asynchronously negated. As soon as the next data is available, it is transferred to the output latches. When H4 is negated, asserted transitions of H3 have no affect on data paths. The H4S status bit is always clear. When H34 enable is clear, H4 is held negated.
5. H4 may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock pulse is generated. But in the case that a subsequent H3 asserted edge occurs before termination of the pulse, H4 is negated asynchronously shortening the pulse. The H4S status bit is always cleared. When H34 enable is clear, H4 is held negated.

The H3S status bit may be programmed for two interpretations:

1. The H3S status bit is set when either the port initial or final output latch can accept new data. It is clear when both latches are full and cannot accept new data.
2. The H3S status bit is set when both of the port output latches are empty. It is clear when at least one latch is full.

The programmable options of the H2 pin are:

1. H2 may be an edge-sensitive input pin independent of H1 and the transfer of port data. On the asserted edge of H2, the H2S status bit is set. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status register (PSR), or when the H12 enable bit of the port general control register is clear.
2. H2 may be a general-purpose output pin that is always negated. The H2S status bit is always clear.
3. H2 may be a general-purpose output pin that is always asserted. The H2S status bit is always clear.

For pins used as inputs, data written to either data register is double buffered and passed to the initial or final output latch, as usual, but the output buffer is disabled (refer to **3.3.2 Submode 01 — Pin-Definable Double-Buffered Output or Non-Latched Input**).

Programmable Options Mode 1 — Port A Submode XX and Port B Submode X1 (Sheet 1 of 2)

PACR 7 6	Port A Submode
0 0	Submode XX

PACR 5 4 3	H2 Control
0 X X	Input pin — edge-sensitive status input, H2S is set on an asserted edge.
1 X 0	Output pin — negated, H2S is always cleared.
1 X 1	Output pin — asserted, H2S is always cleared.

PACR 2	H2 Interrupt Enable
0	The H2 interrupt is disabled.
1	The H2 interrupt is enabled.

PACR 1	H1 SVCRQ Enable
0	The H1 interrupt is disabled.
1	The H1 interrupt is enabled.

PACR 0	H1 Status Control
X	H1 is an edge-sensitive status input. H1S is set by an asserted edge of H1.

PBCR 7 6	Port B Submode
0 0	Submode X1

PBCR 5 4 3	H4 Control
0 X X	Input pin — edge-sensitive status input, H4S is set on an asserted edge.
1 0 0	Output pin — negated, H4S is always cleared.
1 0 1	Output pin — asserted, H4S is always cleared.
1 1 0	Output pin — interlocked input handshake protocol.
1 1 1	Output pin — pulsed input handshake protocol.

PBCR 2	H4 Interrupt Enable
0	The H4 interrupt is disabled.
1	The H4 interrupt is enabled.

Programmable Options Mode 1 — Port A Submode XX
and Port B Submode X1 (Sheet 2 of 2)

PBCR
1 H3 SVCRQ Enable
0 The H3 interrupt and DMA request are disabled.
1 The H3 interrupt and DMA request are enabled.

PBCR
0 H3 Status Control
0 The H3S status bit is set when either the initial or final output latch of ports A and B can accept new data. It is clear when both latches are full and cannot accept new data.
1 The H3S status bit is set when both the initial and final output latches of ports A and B are empty. The H3S status bit is clear when at least one set of output latches is full.

3.5 MODE 2 — BIDIRECTIONAL 8-BIT MODE

In mode 2, port A is used for bit I/O with no associated handshake pins. Port B is used for bidirectional 8-bit double-buffered transfers. H1 and H2, enabled by the H12 enable bit in the port general control register, control output transfers, while H3 and H4, enabled by the port general control register bit H34 enable, control input transfers. The instantaneous direction of the data is determined by the H1 handshake pin. The port B data direction register is not used. The port A and port B submode fields do not affect PI/T operation in mode 2.

3.5.1 Port A Bit I/O (Pin-Definable Single-Buffered Output or Non-Latched Input)

Mode 2, port A performs simple bit I/O with no associated handshake pins. This configuration is intended for applications in which several independent devices must be controlled or monitored. Data written to the port A data register is single buffered. If the port A data direction register bit for that pin is set (output), the output buffer is enabled. If it is zero (input), data written is still latched but not available at the pin. Data read from the data register is either the instantaneous value of the pin (if data is stable from CS asserted to DTACK asserted, data on these pins will be guaranteed valid in the data register) or what was written to the data register, depending on the contents of the port A data direction register. This is summarized in Table 3-3.

Table 3-3. Mode 2 Port A Data Paths

Mode	Read Port A Data Register		Write Port A Data Register	
	DDR = 0	DDR = 1	DDR = 0	DDR = 1
2	Pin	FOL	FOL	FOL, S.B

Abbreviations:
S.B. – Single Buffered
FOL – Final Output Latch
DDR – Data Direction Register

3.5.2 Port B — Double-Buffered Bidirectional Data

The output buffers of port B are controlled by the level of H1. When H1 is negated, the port B output buffers (all eight) are enabled and the pins drive the bidirectional bus. Generally, H1 is negated by the peripheral in response to an asserted H2, which indicates that new output data is present in the double-buffered latches. Following acceptance of the data, the peripheral asserts H1, disabling the port B output buffers. Other than controlling the output buffers, H1 is edge-sensitive as in other modes.

3.5.2.1 DOUBLE-BUFFERED INPUT TRANSFERS. Port B input data that meets the port setup and hold times is latched on the asserted edge of H3 and placed in the initial input latch or the final input latch. H3 is edge-sensitive, and may assume any duty-cycle as long as both high and low minimum times are observed. The PI/T contains a port status register whose H3S status bit is set anytime any input data that has not been read by the bus master is present in the double-buffered latches. The action of H4 is programmable and can be programmed as:

1. H4 may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H3 input. As soon as the input latches become ready, H4 is again asserted. When the input double-buffered latches are full, H4 remains negated until data is removed. Thus, anytime the H4 output is asserted, new input data may be entered by asserting H3. At other times transitions on H3 are ignored. The H4S status bit is always clear. When H34 enable in the port general control register is clear, H4 is held negated.
2. H4 may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock cycle pulse is generated. But in the case that a subsequent H3 asserted edge occurs before termination of the pulse, H4 is negated asynchronously. Thus, anytime after the leading edge of the H4 pulse, new data may be entered in the double-buffered input latches. The H4S status bit is always clear. When H34 enable is clear, H4 is held negated.

3.5.2.2 DOUBLE-BUFFERED OUTPUT TRANSFERS. Data, written by the bus master to the PI/T, is stored in the port's output latch. The peripheral accepts the data by asserting H1, which causes the next data to be moved to the port's output latch as soon as it is available. The H1S status bit, in the port status register, may be programmed for two interpretations. Normally the status bit is a one when there is at least one latch in the double-buffered data path that can accept new data. After writing one byte of data to the ports, an interrupt service routine could check this bit to determine if it could store another byte; thus filling both latches. When the bus master is finished, it is often useful to be able to check whether all of the data has been transferred to the peripheral. The H1S status control bit of the port A control register provides this flexibility. The H1S status bit is set when both output latches are empty. The programmable options for H2 are:

1. H2 may be an output pin in the interlocked output handshake protocol. It is asserted when the port output latches are ready to transfer new data. It is negated asynchronously following the asserted edge of the H1 input. As soon as the output latches become ready, H2 is again asserted. When the output double-buffered latches are full, H2 remains asserted until data is removed. Thus, anytime the H2 output is asserted, new output data may be transferred by asserting H1. At other times transitions on H1 are ignored. The H2S status bit is always clear. When H12 enable in the port general control register is clear, H2 is held negated.
2. H2 may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked input protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock cycle pulse is generated. But in the case that a subsequent H1 asserted edge occurs before termination of the pulse, H2 is negated asynchronously. Thus, anytime after the leading edge of the H2 pulse, new data may be transferred to the double-buffered output latches. The H2S status bit is always clear. When H12 enable is clear, H2 is held negated.

The $\overline{\text{DMAREQ}}$ pin may be associated with either input transfers (H3) or output transfers (H1), but not both. Refer to Table 3-4 for a summary of the port B data register responses in mode 2.

Table 3-4. Mode 2 Port B Data Paths

Mode	Read Port B Data Register	Write Port B Data Register
2	FIL, D.B.	IOL/FOL, D.B.

Abbreviations:
IOL – Initial Output Latch
FOL – Final Output Latch
FIL – Final Input Latch
D.B. – Double Buffered

Programmable Options Mode 2 – Port A Submode XX and Port B Submode XX (Sheet 1 of 2)

PACR
7 6 **Port A Submode**
X X Submode XX

PACR
5 4 3 **H2 Control**
X X 0 Output pin – interlocked output handshake protocol, H2S is always cleared.
X X 1 Output pin – pulsed output handshake protocol, H2S is always cleared.

PACR
2 **H2 Interrupt Enable**
0 The H2 interrupt is disabled.
1 The H2 interrupt is enabled.

PACR
1 **H1 SVCRQ Enable**
0 The H1 interrupt and DMA request are disabled.
1 The H1 interrupt and DMA request are enabled.

PACR
0 **H1 Status Control**
0 The H1 status bit is set when either the port B initial or final output latch can accept new data. It is clear when both latches are full and cannot accept new data.
1 The H1S status bit is set when both of the port B output latches are empty. It is clear when at least one latch is full.

PBCR
7 6 **Port B Submode**
X X Submode XX

PBCR
5 4 3 **H4 Control**
X X 0 Output pin – interlocked input handshake protocol, H4S is always cleared.
X X 1 Output pin – pulsed input handshake protocol, H4S is always cleared.

PBCR
2 **H4 Interrupt Enable**
0 The H4 interrupt is disabled.
1 The H4 interrupt is enabled.

Programmable Options Mode 2 — Port A Submode XX
and Port B Submode XX (Sheet 2 of 2)

PBCR	
1	**H3 SVCRQ Enable**
0	The H3 interrupt and DMA request are disabled.
1	The H3 interrupt and DMA request are enabled.

PBCR	
0	**H3 Status Control**
X	The H3S status bit is set anytime input data is present in the double-buffered input path.

3.6 MODE 3 — BIDIRECTIONAL 16-BIT MODE

In mode 3, ports A and B are used for bidirectional 16-bit double-buffered transfers. H1 and H2 control output transfers, while H3 and H4 control input transfers. H1 and H2 are enabled by the H12 enable bit while H3 and H4 are enabled by the H34 enable bit of the port general control register. The instantaneous direction of data is determined by the H1 handshake pin, thus, the data direction registers are not used and have no affect. The port A and port B submode fields do not affect PI/T operation in mode 3. Port A and port B output buffers are controlled by the level of H1. When H1 is negated, the output buffers (all 16) are enabled and the pins drive the bidirectional port bus. Generally a peripheral will negate H1 in response to an asserted H2, which indicates that new output data is present in the double-buffered latches. Following acceptance of the data, the peripheral asserts H1, disabling the output buffers. Other than controlling the output buffers, H1 is edge-sensitive as in other modes. The port A and port B data direction registers are not used.

3.6.1 Double-Buffered Input Transfers

Port A and B input data that meets the port setup and hold times is latched on the asserted edge of H3 and placed in the initial input latch or the final input latch. H3 is edge-sensitive, and may assume any duty-cycle as long as both high and low minimum times are observed. The PI/T contains a port status register whose H3S status bit is set anytime any input data is present in the double-buffered latches that has not been read by the bus master. The action of H4 is programmable and can be programmed as:

1. H4 may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H3 input. As soon as the input latches become ready, H4 is again asserted. When the input double-buffered latches are full, H4 remains negated until data is removed. Thus, anytime the H4 output is asserted, new input data may be entered by asserting H3. At other times transitions on H3 are ignored. The H4S status bit is always clear. When H34 enable in the port general control register is clear, H4 is held negated.
2. H4 may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock cycle pulse is generated. But in the case that a subsequent H3 asserted edge occurs before termination of the pulse, H4 is negated asynchronously. Thus, anytime after the leading edge of the H4 pulse, new data may be entered in the double-buffered input latches. The H4 status bit is always clear. When H34 enable is clear, H4 is held negated.

3.6.2 Double-Buffered Output Transfers

Data, written by the bus master to the PI/T, is stored in the port's output latch. The peripheral accepts the data by asserting H1, which causes the next data to be moved to the port's output latch as soon as it is available. The H1S status bit, in the port status register, may be programmed for two interpretations. Normally the status bit is a one when there is at least one latch in the double-buffered data path that can accept new data. After writing one byte of data to the ports, an interrupt service routine could check this bit to determine if it could store another byte; thus filling both latches. When the bus master is finished, it is often useful to be able to check whether all of the data has been transferred to the peripheral. The H1S status control bit of the port A control register provides this flexibility. The H1S status bit is set when both output latches are empty. The programmable options for H2 are:

1. H2 may be an output pin in the interlocked output handshake protocol. It is asserted when the port output latches are ready to transfer new data. It is negated asynchronously following the asserted edge of the H1 input. As soon as the output latches become ready, H2 is again asserted. When the output double-buffered latches are full, H2 remains asserted until data is removed. Thus, anytime the H2 output is asserted, new output data may be transferred by asserting H1. At other times transitions on H1 are ignored. The H2S status bit is always clear. When H12 enable in the port general control register is clear, H2 is held negated.
2. H2 may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked output protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock pulse is generated. But in the case that a subsequent H1 asserted edge occurs before termination of the pulse, H2 is negated asynchronously shortening the pulse. The H2S status bit is always zero. When H12 enable is zero, H2 is held negated.

Mode 3 can provide convenient high-speed 16-bit transfers. The port A and B data registers are addressed for compatibility with the MC68000's move peripheral (MOVEP) instruction and with the MC68450 DMAC. To take advantage of this, port A should contain the most significant data and always be read or written by the bus master first. The interlocked and pulsed handshake protocols, status bits, and $\overline{\text{DMAREQ}}$ are keyed to the access of port B data register in mode 3. If it is accessed last, the 16-bit double-buffered transfer proceeds smoothly.

The $\overline{\text{DMAREQ}}$ pin may be associated with either input transfers (H3) or output transfers (H1), but not both. Refer to Table 3-5 for a summary of the port A and B data paths in mode 3.

Table 3-5. Mode 3 Port A and B Data Paths

Mode	Read Port A and B Data Register	Write Port A and B Data Register
3	FIL, D.B.	IOL/FOL, D.B., Note 1
Note 1: Data written to Port A goes to a temporary latch. When the Port B data register is later written, Port A data is transferred to IOL/FOL.		
Abbreviations: IOL – Initial Output Latch FOL – Final Output Latch FIL – Final Input Latch		S.B – Single Buffered D.B. – Double Buffered

Programmable Options Mode 3 — Port A Submode XX and Port B Submode XX

PACR
7 6 **Port A Submode**
X X Submode XX

PACR
5 4 3 **H2 Control**
X X 0 Output pin — interlocked output handshake protocol, H2S status always cleared.
X X 1 Output pin — pulsed output handshake protocol, H2S status always cleared.

PACR
2 **H2 Interrupt Enable**
0 The H2 interrupt is disabled.
1 The H2 interrupt is enabled.

PACR
1 **H1 SVCRQ Enable**
0 The H1 interrupt and DMA request are disabled.
1 The H1 interrupt and DMA request are enabled.

PACR
0 **H1 Status Control**
0 The H1 status bit is set when either the port B initial or final output latch can accept new data. It is clear when both latches are full and cannot accept new data.
1 The H1S status bit is set when both of the port B output latches are empty. It is clear when at least one latch is full.

PBCR
7 6 **Port B Submode**
X X Submode XX

PBCR
5 4 3 **H4 Control**
X X 0 Output pin — interlocked input handshake protocol, H4S is always clear.
X X 1 Output pin — pulsed input handshake, H4S is always clear.

PBCR
2 **H4 Interrupt Enable**
0 The H4 interrupt is disabled.
1 The H4 interrupt is enabled.

PBCR
1 **H3 SVCRQ Enable**
0 The H3 interrupt and DMA request are disabled.
1 The H3 interrupt and DMA request are enabled.

PBCR
0 **H3 Status Control**
X The H3S status bit is set anytime input data is present in the double-buffered input path.

SECTION 4
PROGRAMMER'S MODEL

This section describes the internal accessible register organization as represented in Table 1-3 located on foldout pages 1 and 2 at the end of this document and in Table 4-1. Address space within the address map is reserved for future expansion.

Table 4-1. PI/T Register Addressing Assignments

Register		Register Select Bits 5	4	3	2	1	Accessible	Affected by Reset	Affected by Read Cycle
Port General Control Register	(PGCR)	0	0	0	0	0	R W	Yes	No
Port Service Request Register	(PSRR)	0	0	0	0	1	R W	Yes	No
Port A Data Direction Register	(PADDR)	0	0	0	1	0	R W	Yes	No
Port B Data Direction Register	(PBDDR)	0	0	0	1	1	R W	Yes	No
Port C Data Direction Register	(PCDDR)	0	0	1	0	0	R W	Yes	No
Port Interrupt Vector Register	(PIVR)	0	0	1	0	1	R W	Yes	No
Port A Control Register	(PACR)	0	0	1	1	0	R W	Yes	No
Port B Control Register	(PBCR)	0	0	1	1	1	R W	Yes	No
Port A Data Register	(PADR)	0	1	0	0	0	R W	No	**
Port B Data Register	(PBDR)	0	1	0	0	1	R W	No	**
Port A Alternate Register	(PAAR)	0	1	0	1	0	R	No	No
Port B Alternate Register	(PBAR)	0	1	0	1	1	R	No	No
Port C Data Register	(PCDR)	0	1	1	0	0	R W	No	No
Port Status Register	(PSR)	0	1	1	0	1	R W*	Yes	No
Timer Control Register	(TCR)	1	0	0	0	0	R W	Yes	No
Timer Interrupt Vector Register	(TIVR)	1	0	0	0	1	R W	Yes	No
Counter Preload Register High	(CPRH)	1	0	0	1	1	R W	No	No
Counter Preload Register Middle	(CPRM)	1	0	1	0	0	R W	No	No
Counter Preload Register Low	(CPRL)	1	0	1	0	1	R W	No	No
Count Register High	(CNTRH)	1	0	1	1	1	R	No	No
Count Register Middle	(CNTRM)	1	1	0	0	0	R	No	No
Count Register Low	(CNTRL)	1	1	0	0	1	R	No	No
Timer Status Register	(TSR)	1	1	0	1	0	R W*	Yes	No

*A write to this register may perform a special status resetting operation.
**Mode dependent.
R = Read
W = Write

Throughout this section the following conventions are maintained:

1. A read from a reserved location in the map results in a read from the "null register." The null register returns all zeros for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle, but written data is ignored.
2. Unused bits of a defined register are denoted by "*" and are read as zeros; written data is ignored.

3. Bits that are unused in the chosen mode/submode but are used in others are denoted by "X", and are readable and writable. Their content, however, is ignored in the chosen mode/submode.
4. All registers are addressable as 8-bit quantities. To facilitate operation with the MOVEP instruction and the DMAC, addresses are ordered such that certain sets of registers may also be accessed as words (two bytes) or long words (four bytes).

4.1 PORT GENERAL CONTROL REGISTER (PGCR)

Port General Control Register (PGCR)

7	6	5	4	3	2	1	0
Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense

The port general control register controls many of the functions that are common to the overall operation of the ports. The PGCR is composed of three major fields: bits 7 and 6 define the operational mode of ports A and B and affect operation of the handshake pins and status bits; bits 5 and 4 allow a software-controlled disabling of particular hardware associated with the handshake pins of each port; and bits 3-0 define the sense of the handshake pins. The PGCR is always readable and writable.

All bits are reset to zero when the $\overline{\text{RESET}}$ pin is asserted.

The port mode control field should be altered only when the H12 enable and H34 enable bits are zero. Except when mode zero is desired (submode 1X), the port general control register should be written once to establish the mode with the H12 and H34 bits clear. Any other necessary control registers can then be programmed, after which H12 or H34 is set. In order to enable the respective operation(s), the port general control register should be written again.

PGCR
7 6 Port Mode Control

0 0 Mode 0 (Unidirectional 8-Bit Mode)
0 1 Mode 1 (Unidirectional 16-Bit Mode)
1 0 Mode 2 (Bidirectional 8-Bit Mode)
1 1 Mode 3 (Bidirectional 16-Bit Mode)

PGCR
5 H34 Enable

0 Disabled
1 Enabled

PGCR
4 H12 Enable

0 Disabled
1 Enabled

PGCR
3-0 Handshake Pin Sense

0 The associated pin is at the high-voltage level when negated and at the low-voltage level when asserted.
1 The associated pin is at the low-voltage level when negated and at the high-voltage level when asserted.

4.2 PORT SERVICE REQUEST REGISTER (PSRR)

Port Service Request Register (PSRR)

7	6 5	4 3	2 1 0
*	SVCRQ Select	Operation Select	Port Interrupt Priority Control

The port service request register controls other functions that are common to the overall operation to the ports. It is composed of four major fields: bit 7 is unused and is always read as zero; bits 6 and 5 define whether interrupt or DMA requests are generated from activity on the H1 and H3 handshake pins; bits 4 and 3 determine whether two dual-function pins operate as port C or port interrupt request/acknowledge pins; and bits 2, 1, and 0 control the priority among all port interrupt sources. Since bits 2, 1, and 0 affect interrupt operation, it is recommended that they be changed only when the affected interrupt(s) is (are) disabled or known to remain inactive. The PSRR is always readable and writable.

All bits are reset to zero when the $\overline{\text{RESET}}$ pin is asserted.

PSRR 6 5 — SVCRQ Select

0 X The PC4/$\overline{\text{DMAREQ}}$ pin carries the PC4 function; DMA is not used.

PSRR — SVCRQ Select

1 0 The PC4/$\overline{\text{DMAREQ}}$ pin carries the $\overline{\text{DMAREQ}}$ function and is associated with double-buffered transfers controlled by H1. H1 is removed from the PI/T's interrupt structure, and thus, does not cause interrupt requests to be generated. To obtain $\overline{\text{DMAREQ}}$ pulses, port A control register bit 1 (H1 SVCRQ enable) must be a one.

1 1 The PC4/$\overline{\text{DMAREQ}}$ pin carries the $\overline{\text{DMAREQ}}$ function and is associated with double-buffered transfers controlled by H3. H3 is removed from the PI/T's interrupt structure, and thus, does not cause interrupt requests to be generated. To obtain $\overline{\text{DMAREQ}}$ pulses, port B control register bit 1 (H3 SVCRQ enable) must be one.

PSRR 4 3 — Interrupt Pin Function Select

0 0 The PC5/$\overline{\text{PIRQ}}$ pin carries the PC5 function, no interrupt support.
The PC6/$\overline{\text{PIACK}}$ pin carries the PC6 function, no interrupt support.

0 1 The PC5/$\overline{\text{PIRQ}}$ pin carries the $\overline{\text{PIRQ}}$ function, supports autovectored interrupts.
The PC6/$\overline{\text{PIACK}}$ pin carries the PC6 function, supports autovectored interrupts.

1 0 The PC5/$\overline{\text{PIRQ}}$ pin carries the PC5 function.
The PC6/$\overline{\text{PIACK}}$ pin carries the $\overline{\text{PIACK}}$ function.

1 1 The PC5/$\overline{\text{PIRQ}}$ pin carries the $\overline{\text{PIRQ}}$ function, supports vectored interrupts.
The PC6/$\overline{\text{PIACK}}$ pin carries the $\overline{\text{PIACK}}$ function, supports vectored interrupts.

Bits 2, 1, and 0 determine port interrupt priority. The priority as shown in Table 4-2 is in descending order left to right.

Table 4-2. PSRR Port Interrupt Priority Control

2 1 0	Highest			Lowest
0 0 0	H1S	H2S	H3S	H4S
0 0 1	H2S	H1S	H3S	H4S
0 1 0	H1S	H2S	H4S	H3S
0 1 1	H2S	H1S	H4S	H3S

2 1 0	Highest			Lowest
1 0 0	H3S	H4S	H1S	H2S
1 0 1	H3S	H4S	H2S	H1S
1 1 0	H4S	H3S	H1S	H2S
1 1 1	H4S	H3S	H2S	H1S

4.3 PORT DATA DIRECTION REGISTERS

The following paragraphs describe the port data direction registers.

4.3.1 Port A Data Direction Register (PADDR)

The port A data direction register determines the direction and buffering characteristics of each of the port A pins. One bit in the PADDR is assigned to each pin. A zero indicates that the pin is used as a input, while a one indicates it is used as an output. The PADDR is always readable and writable. This register is ignored in mode 3.

All bits are reset to the zero (input) state when the $\overline{\text{RESET}}$ pin is asserted.

4.3.2 Port B Data Direction Register (PBDDR)

The PBDDR is identical to the PADDR for the port B pins and the port B data register, except that this register is ignored in modes 2 and 3.

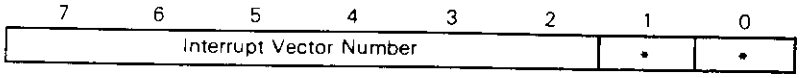
4.3.3 Port C Data Direction Register (PCDDR)

The port C data direction register specifies whether each dual-function pin that is chosen for port C operation is an input (zero) or an output (one) pin. The PCDDR, along with bits that determine the respective pin's function, also specify the exact hardware to be accessed at the port C data register address (see **4.6.3 Port C Data Register (PCDR)** for more details). The PCDDR is an 8-bit register that is readable and writable at all times. Its operation is independent of the chosen PI/T mode.

These bits are cleared to zero when the $\overline{\text{RESET}}$ pin is asserted.

4.4 PORT INTERRUPT VECTOR REGISTER (PIVR)

Port Interrupt Vector Register (PIVR)



The port interrupt vector register contains the upper order six bits of the four port interrupt vectors. The contents of this register may be read two ways: by an ordinary read cycle, or by a port interrupt acknowledge bus cycle. The exact data read depends on how the cycle was initiated and other factors. Behavior during a port interrupt acknowledge cycle is summarized in Table 2-1.

From a normal read cycle, there is never a consequence to reading this register. Following negation of the $\overline{\text{RESET}}$ pin, but prior to writing to the PIVR, a $0F will be read. After writing to the register, the upper six bits may be read and the lower two bits are forced to zero. No prioritization computation is performed.

4.5 PORT CONTROL REGISTERS (PACR, PBCR)

The port A and B control registers (PACR and PBCR) are described in **SECTION 3 PORT MODES.** The description is organized such that for each mode/submode all programmable options of each pin and status bit are given.

4.6 PORT DATA REGISTERS

The following paragraphs describe the port data registers.

4.6.1 Port A Data Register (PADR)

The port A data register is a holding register for moving data to and from the port A pins. The port A data direction register determines whether each pin is an input (zero) or an output (one), and is used in configuring the actual data paths. The data paths are described in **SECTION 3 PORT MODES.**

This register is readable and writable at all times. Depending on the chosen mode/submode, reading or writing may affect the double-buffered handshake mechanism. The port A data register is not affected by the assertion of the $\overline{\text{RESET}}$ pin.

4.6.2 Port B Data Register (PBDR)

The port B data register is a holding register for moving data to and from port B pins. The port B data direction register determines whether each pin is an input (zero) or an output (one), and is used in configuring the actual data paths. The data paths are described in **SECTION 3 PORT MODES.**

This register is readable and writable at all times. Depending on the chosen mode/submode, reading or writing may affect the double-buffered handshake mechanism. The port B data register is not affected by the assertion of the $\overline{\text{RESET}}$ pin.

4.6.3 Port C Data Register (PCDR)

The port C data register is a holding register for moving data to and from each of the eight port C/alternate-function pins. The exact hardware accessed is determined by the type of bus cycle (read or write) and individual conditions affecting each pin. These conditions are: 1) whether the pin is used for the port C or alternate function, and 2) whether the port C data direction register indicates the input or output direction. The port C data register is single buffered for output pins and non-latched for input pins. These conditions are summarized in Table 4-3.

Table 4-3. PCDR Hardware Accesses

Operation	Port C Function		Alternate Function	
	PCDDR = 0	PCDDR = 1	PCDDR = 0	PCDDR = 1
Read Port C Data Register	Pin	Output Register	Pin	Output Register
Write Port C Data Register	Output Register, Buffer Disabled	Output Register, Buffer Enabled	Output Register	Output Register

Note that two additional useful benefits result from this structure. First, it is possible to directly read the state of a dual-function pin while used for the non-port C function. Second, it is possible to generate program controlled transitions on alternate-function pins by switching back to the port C function and writing to the PCDR.

This register is readable and writable at all times and operation is independent of the chosen PI/T mode. The port C data register is not affected by the assertion of the $\overline{\text{RESET}}$ pin.

4.7 PORT ALTERNATE REGISTERS

The following paragraphs describe the port alternate registers.

4.7.1 Port A Alternate Register (PAAR)

The port A alternate register is an alternate register for reading the port A pins. It is a read-only address and no other PI/T condition is affected. In all modes, the instantaneous pin level is read and no input latching is performed except at the data bus interface. Writes to this address are answered with $\overline{DTACK}$, but the data is ignored.

4.7.2 Port B Alternate Register (PBAR)

The port B alternate register is an alternate register for reading the port B pins. It is a read-only address and no other PI/T condition is affected. In all modes, the instantaneous pin level is read and no input latching is performed except at the data bus interface. Writes to this address are answered with $\overline{DTACK}$, but the data is ignored.

4.8 PORT STATUS REGISTER (PSR)

Port Status Register (PSR)

7	6	5	4	3	2	1	0
H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S

The port status register contains information about handshake pin activity. Bits 7-4 show the instantaneous level of the respective handshake pin, and are independent of the handshake pin sense bits in the port general control register. Bits 3-0 are the respective status bits referred to throughout this document. Their interpretation depends on the programmed mode/submode of the PI/T. For bits 3-0 a one is the active or asserted state.

4.9 TIMER CONTROL REGISTER (TCR)

Timer Control Register (TCR)

7	6	5	4	3	2	1	0
TOUT/$\overline{TIACK}$ Control			Z. D. Control	*	Clock Control		Timer Enable

The timer control register (TCR) determines all operations of the timer. Bits 7-5 configure the PC3/TOUT and PC7/$\overline{TIACK}$ pins for port C, square wave, vectored interrupt, or autovectored interrupt operation; bit 4 specifies whether the counter receives data from the counter preload register or continues counting when zero detect is reached; bit 3 is unused and is read as zero; bits 2 and 1 configure the path from the CLK and TIN pins to the counter controller; and bit 0 enables the timer. This register is readable and writable at all times. All bits are cleared to zero when the $\overline{RESET}$ pin is asserted.

TCR 7 6 5	TOUT/TIACK Control
0 0 X	The dual-function pins PC3/TOUT and PC7/$\overline{TIACK}$ carry the port C function.
0 1 X	The dual-function pin PC3/TOUT carries the TOUT function. In the run state it is used as a square-wave output and is toggled on zero detect. The TOUT pin is high while in the halt state. The dual-function pin PC7/$\overline{TIACK}$ carries the PC7 function.

1 0 0 The dual-function pin PC3/TOUT carries the TOUT function. In the run or halt state it is used as a timer interrupt request output. The timer interrupt is disabled; thus, the pin is always three stated. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the $\overline{\text{TIACK}}$ function; however, since interrupt request is negated, the PI/T produces no response (i.e:, no data or DTACK) to an asserted $\overline{\text{TIACK}}$. Refer to **5.1.3 Timer Interrupt Acknowledge Cycles** for details.

1 0 1 The dual-function pin PC3/TOUT carries the TOUT function and is used as a timer interrupt request output. The timer interrupt is enabled; thus, the pin is low when the timer ZDS status bit is one. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the $\overline{\text{TIACK}}$ function and is used as a timer interrupt acknowledge input. Refer to the **5.1.3 Timer Interrupt Acknowledge Cycles** for details. This combination supports vectored timer interrupts.

1 1 0 The dual-function pin PC3/TOUT carries the TOUT function. In the run or halt state it is used as a timer interrupt request output. The timer interrupt is disabled; thus, the pin is always three-stated. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the PC7 function.

1 1 1 The dual-function pin PC3/TOUT carries the TOUT function and is used as a timer interrupt request output. The timer interrupt is enabled; thus, the pin is low when the timer ZDS status bit is one. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the PC7 function and autovectored interrupts are supported.

TCR 4 **Zero Detect Control**

0 The counter is loaded from the counter preload register on the first clock to the 24-bit counter after zero detect, then resumes counting.

1 The counter rolls over on zero detect, then continues counting.

TCR 3 Unused and is always read as zero.

TCR 2 1 **Clock Control**

0 0 The PC2/TIN input pin carries the port C function, and the CLK pin and prescaler are used. The prescaler is decremented on the falling transition of the CLK pin; the 24-bit counter is decremented, rolls over, or is loaded from the counter preload registers when the prescaler rolls over from $00 to $1F. The timer enable bit determines whether the timer is in the run or halt state.

0 1 The PC2/TIN pin serves as a timer input, and the CLK pin and prescaler are used. The prescaler is decremented on the falling transition of the CLK pin; the 24-bit counter is decremented, rolls over, or is loaded from the counter preload registers when the prescaler rolls over from $00 to $1F. The timer is in the run state when the timer enable bit is one and the TIN pin is high; otherwise, the timer is in the halt state.

1 0 The PC2/TIN pin serves as a timer input and the prescaler is used. The prescaler is decremented following the rising transition of the TIN pin after being synchronized with the internal clock. The 24-bit counter is decremented, rolls over, or is loaded from the counter preload registers when the prescaler rolls over from $00 to $1F. The timer enable bit determines whether the timer is in the run or halt state.

1 1 The PC2/TIN pin serves as a timer input and the prescaler is not used. The 24-bit counter is decremented, rolls over, or is loaded from the counter preload registers following the rising edge of the TIN pin after being synchronized with the internal clock. The timer enable bit determines whether the timer is in the run or halt state.

TCR 0 **Timer Enable**

0 Disabled

1 Enabled

4.10 TIMER INTERRUPT VECTOR REGISTER (TIVR)

The timer interrupt vector register contains the 8-bit vector supplied when the timer interrupt acknowledge pin $\overline{\text{TIACK}}$ is asserted. The register is readable and writable at all times, and the same value is always obtained from a normal read cycle or a timer interrupt acknowledge bus cycle ($\overline{\text{TIACK}}$). When the $\overline{\text{RESET}}$ pin is asserted the value of $0F is loaded into the register. Refer to **5.1.3 Timer Interrupt Acknowledge Cycles** for more details.

4.11 COUNTER PRELOAD REGISTER H, M, L (CPRH-L)

Counter Preload Register H, M, L (CPRH-L)

7	6	5	4	3	2	1	0	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	CPRH
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	CPRM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CPRL

The counter preload registers are a group of three 8-bit registers used for storing data to be transferred to the counter. Each of the registers is individually addressable, or the group may be accessed with the MOVEP.L or the MOVEP.W instructions. The address $12 (one less than the address of CPRH) is the null register and is reserved so that zeros are read in the upper eight bits of the destination data register when a MOVEP.L is used. Data written to this address is ignored.

These registers are readable and writable at all times. A read cycle proceeds independently of any transfer to the counter, which may be occurring simultaneously. To insure proper operation of the PI/T timer, a value of $000000 may not be stored in the counter preload registers for use with the counter. The $\overline{\text{RESET}}$ pin does not affect the contents of these registers.

4.12 COUNT REGISTER H, M, L (CNTRH-L)

Count Register H, M, L (CNTRH-L)

7	6	5	4	3	2	1	0	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	CNTRH
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	CNTRM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CNTRL

The count registers are a group of three 8-bit addresses at which the counter can be read. The contents of the counter are not latched during a read bus cycle; thus, the data read at these addresses is not guaranteed if the timer is in the run state. Write operations to these addresses result in a normal bus cycle but the data is ignored.

Each of the registers is individually addressable, or the group may be accessed with the MOVEP.L or the MOVEP.W instructions. The address, one less than the address CNTRH, is the null register and is reserved so that zeros are read in the upper eight bits of the destination data register when a MOVEP.L is used. Data written to this address is ignored.

4.13 TIMER STATUS REGISTER (TSR)

Timer Status Register (TSR)

7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	ZDS

The timer status register contains one bit from which the zero detect status can be determined. The ZDS status bit (bit 0) is an edge-sensitive flip-flop that is set to one when the 24-bit counter decrements from $000001 to $000000. The ZDS status bit is cleared to zero following the direct reset operation or when the timer is halted. Note that when the $\overline{\text{RESET}}$ pin is asserted the timer is disabled, and thus enters the halt state.

This register is always readable without consequence. A write access performs a direct reset operation if bit 0 in the written data is one. Following that, the ZDS bit is zero.

This register is constructed with a reset dominant S-R flip-flop so that all clearing conditions prevail over the possible zero detect condition.

Bits 7-1 are unused and are read as zero.

4.14 REGISTER VALUE AFTER RESET

Table 1-3, located on foldout pages 1 and 2 at the end of this document, shows the values that remain or are changed after a reset. Note that interrupt vector registers are initialized to $0F. For the port interrupt vector register, the only time that bits 0 and 1 are set is after reset.

SECTION 5
TIMER OPERATION AND APPLICATIONS SUMMARY

This section describes the programmable options available, capabilities, and restrictions that apply to the timer. Programming of the timer control register is outlined with several examples given.

5.1 TIMER OPERATION

The MC68230 timer can provide several facilities needed by M68000 operating systems. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. Also, it can be used for elapsed time measurement or as a device watchdog.

The PI/T timer contains a 24-bit synchronous down counter that is loaded from three 8-bit counter preload registers. The 24-bit counter may be clocked by the output of a 5-bit (divide-by-32) prescaler or by an external timer input (TIN). If the prescaler is used, it may be clocked by the system clock (CLK pin) or by the TIN external input. The counter signals the occurrence of an event primarily through zero detection. (A zero is when the counter of the 24-bit timer is equal to zero.) This sets the zero detect status (ZDS) bit in the timer status register. It may be checked by the processor or may be used to generate a timer interrupt. The ZDS bit can be reset by writing a one to the timer status register in that bit position independent of timer operation.

The general operation of the timer is flexible and easily programmable. The timer is fully configured and controlled by programming the 8-bit timer control register (refer to **4.9 TIMER CONTROL REGISTER (TCR)** for additional information). It controls: 1) the choice between the port C operation and the timer operation of three timer pins, 2) whether the counter is loaded from the counter preload register or rolls over when zero detect is reached, 3) the clock input, 4) whether the prescaler is used, and 5) whether the timer is enabled.

5.1.1 Run/Halt Definition

The overall operation of the timer is described in terms of the run or halt states. The control of the current state is determined by programming the timer control register. When in the halt state, all of the following occur:

1. The prior content of the counter is not altered and is reliably readable via the count registers.
2. The prescaler is forced to $1F whether or not it is used.
3. The ZDS status bit is forced to zero, regardless of the possible zero contents of the 24-bit counter.

The run state is characterized by:

1. The counter is clocked by the source programmed in the timer control register.
2. The counter is not reliably readable.
3. The prescaler is allowed to decrement if programmed for use.
4. The ZDS status bit is set when the 24-bit counter transitions from $000001 to $000000.

5.1.2 Timer Rules

The following is a set of rules that allow easy application of the timer.

1. Refer to **5.1.1 Run/Halt Definition**.
2. When the $\overline{\text{RESET}}$ pin is asserted, all bits of the timer control register are cleared, configuring the dual function pins as port C inputs.
3. The contents of the counter preload registers and counter are not affected by the $\overline{\text{RESET}}$ pin.
4. The count registers provide a direct read data path from each portion of the 24-bit counter, but data written to their addresses is ignored. (This results in a normal bus cycle.) These registers are readable at any time, but their contents are never latched. Unreliable data may be read when the timer is in the run state.
5. The counter preload registers are readable and writable at any time and this occurs independently of any timer operation. No protection mechanisms are provided against ill-timed writes.
6. The input frequency to the 24-bit counter from the TIN pin or prescaler output must be between zero and the input frequency at the CLK pin divided by eight, regardless of the configuration chosen.
7. For configurations in which the prescaler is used (with the CLK pin or TIN pin as an input), the contents of the counter preload register (CPR) is transferred to the counter the first time that the prescaler passes from $00 to $1F (rolls over) after entering the run state. Thereafter, the counter decrements, rolls over, or is loaded from the counter preload register each time the prescaler rolls over.
8. For configurations in which the prescaler is not used, the contents of the counter preload registers are transferred to the counter on the first asserted edge of the TIN input after entering the run state. On subsequent asserted edges the counter decrements, rolls over, or is loaded from the counter preload registers.
9. The smallest value allowed in the counter preload register for use with the counter is $000001.

5.1.3 Timer Interrupt Acknowledge Cycles

Several conditions may be present when the timer interrupt acknowledge pin ($\overline{\text{TIACK}}$) is asserted. These conditions affect the PI/T's response and the termination of the bus cycle (see Table 5-1).

Table 5-1. Response to Timer Interrupt Acknowledge

PC3/TOUT Function	Response to Asserted $\overline{\text{TIACK}}$
PC3 – Port C Pin	No Response No $\overline{\text{DTACK}}$
TOUT – Square Wave	No Response No $\overline{\text{DTACK}}$
TOUT – Negated Timer Interrupt Request	No Response No $\overline{\text{DTACK}}$
TOUT – Asserted Timer Interrupt Request	Timer Interrupt Vector Contents $\overline{\text{DTACK}}$ Asserted

5.2 TIMER APPLICATIONS SUMMARY

The following paragraphs outline programming of the timer control register for several typical examples.

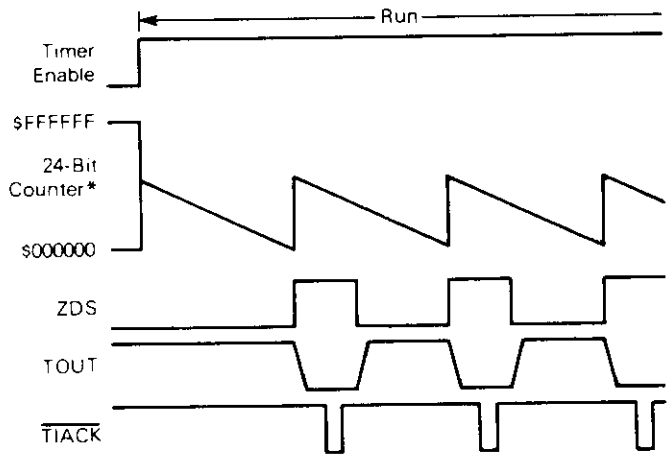
5.2.1 Periodic Interrupt Generator Example

Periodic Interrupt Generator Example

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z.D. Control	*	Clock Control		Timer Enable
1	X	1	0	0	00 or 1X		Changed

In this configuration the timer generates a periodic interrupt. The TOUT pin is connected to the system's interrupt request circuitry and the $\overline{\text{TIACK}}$ pin may be used as an interrupt acknowledge input to the timer. The TIN pin may be used as a clock input.

The processor loads the counter preload registers (CPR) and timer control register (TCR), and then enables the timer. When the 24-bit counter passes from $000001 to $000000, the ZDS status bit is set and the TOUT (interrupt request) pin is asserted. At the next clock to the 24-bit counter, it is again loaded with the contents of the CPRs and thereafter decrements. In normal operation, the processor must direct clear the status bit to negate the interrupt request (see Figure 5-1).



* Analog representation of counter value.

Figure 5-1. Periodic Interrupt Generator Example

5.2.2 Square Wave Generator

Square Wave Generator

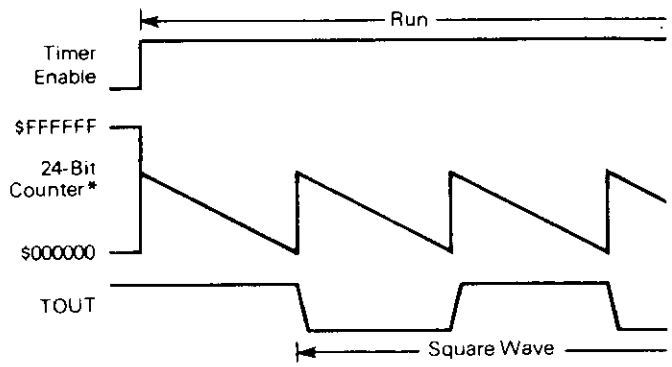
7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Control	*	Clock Control		Timer Enable
0	1	X	0	0	00 or 1X		Changed

In this configuration the timer produces a square wave at the TOUT pin. The TOUT pin is connected to the user's circuitry and the $\overline{\text{TIACK}}$ pin is not used. The TIN pin may be used as a clock input.

The processor loads the counter preload registers and timer control register, and then enables the timer. When the 24-bit counter passes from $000001 to $000000 the ZDS status bit is set and the

TOUT (square wave output) pin is toggled. At the next clock to the 24-bit counter it is again loaded with the contents of the CPRs, and thereafter decrements. In this application there is no need for the processor to direct clear the ZDS status bit; however, it is possible for the processor to sync itself with the square wave by clearing the ZDS status bit, then polling it. The processor may also read the TOUT level at the port C address.

Note that the PC3/TOUT pin functions as PC3 following the negation of $\overline{\text{RESET}}$. If used in the square wave configuration, a pullup resistor may be required to keep a known level prior to programming. Prior to enabling the timer, TOUT is high (see Figure 5-2).



* Analog representation of counter value.

Figure 5-2. Square Wave Generator Example

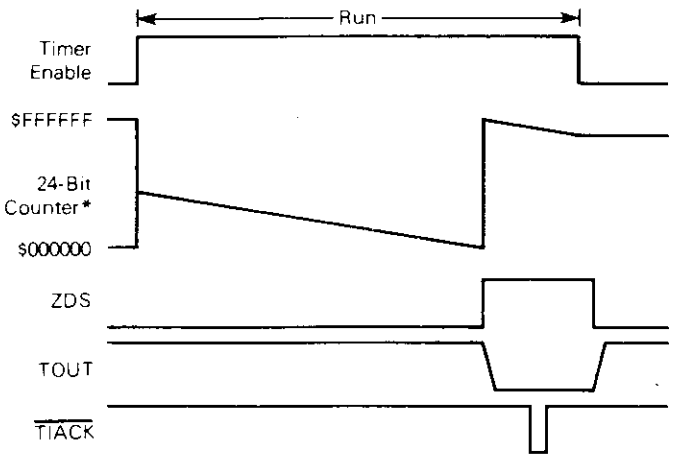
5.2.3 Interrupt After Timeout

Interrupt After Timeout

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Control	*	Clock Control		Timer Enable
1	X	1	1	0	00 or 1X		Changed

In this configuration the timer generates an interrupt after a programmed time period has expired. The TOUT pin is connected to the system's interrupt request circuitry and the $\overline{\text{TIACK}}$ pin may be an interrupt acknowledge input to the timer. The TIN pin may be used as a clock input.

This configuration is similar to the periodic interrupt generator except that the zero detect control bit is set. This forces the counter to roll over after zero detect is reached, rather than reloading from the CPRs. When the processor takes the interrupt it can halt the timer, read the counter and calculate the time from the interrupt request to entering the service routine. Accurate knowledge of the interrupt latency may be useful in some applications (see Figure 5-3).



* Analog representation of counter value.

Figure 5-3. Single Interrupt After Timeout Example

5.2.4 Elapsed Time Measurement Examples

Elapsed time measurement takes several forms; two forms are described in the following paragraphs.

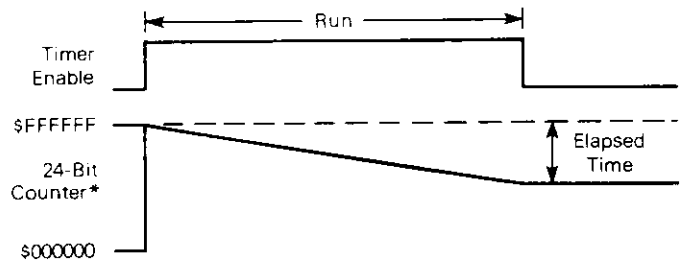
5.2.4.1 SYSTEM CLOCK EXAMPLE. This configuration allows time interval measurement by software. The TIN pin may be used as an external timer enable if desired.

System Clock Example

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Control	*	Clock Control		Timer Enable
0	0	X	1	0	0	0	Changed

The processor loads the counter preload registers (generally with all ones), loads the timer control register, and then enables the timer. The counter is allowed to decrement until the ending event takes place. When it is desired to read the time interval, the processor must halt the timer and then read the counter. If TIN is used as an enable, the start and stop counter functions are controlled externally.

For applications in which the interval may exceed the programmed time interval, zero detection can be counted by polling the status register or through interrupts to simulate additional timer bits. Note that the ZDS bit is latched and should be cleared after each detection of zero. At the end, the timer can be halted and read (see Figure 5-4).



* Analog representation of counter value.

Figure 5-4. Elapsed Time Measurement Example

5.2.4.2 EXTERNAL CLOCK. This configuration allows measurement (counting) of the number of input pulses occurring in an interval in which the counter is enabled. The TIN input pin provides the input pulses. Generally the TOUT and $\overline{\text{TIACK}}$ pins are not used.

External Clock

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Control	*	Clock Control		Timer Enable
0	0	X	1	0	1	X	Changed

This configuration is similar to the elapsed time measurement/system clock configuration except that the TIN pin is used to provide the input frequency. It can be connected to a simple oscillator and the same methods could be used. Alternately, it could be gated off and on externally and the number of cycles occurring while in the run state can be counted. However, minimum pulse width high and low specifications must be met.

5.2.5 Device Watchdog

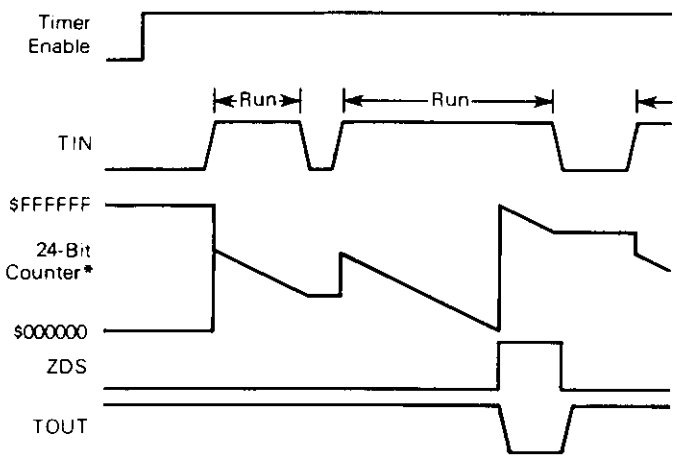
Device Watchdog Example

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Control	*	Clock Control		Timer Enable
1	X	1	1	0	0	1	Changed

This configuration provides the watchdog function needed in many systems. The TIN pin is the timer input whose period at the high (one) level is to be checked. Once allowed by the processor, the TIN input pin controls the run/halt mode. The TOUT pin is connected to external circuitry requiring notification when the TIN pin has been asserted longer than the programmed time. The $\overline{\text{TIACK}}$ pin (timer interrupt acknowledge) is only needed if the TOUT pin is connected to the interrupt circuitry.

The processor loads the counter preload register and timer control register, and then enables the timer. When the TIN input is asserted (one, high) the timer transfers the contents of the counter preload register to the counter and begins counting. If the TIN input is negated before zero detect is reached, the TOUT output and the ZDS status bit remain negated. If zero detect is reached while the TIN input is still asserted, the ZDS status bit is set and the TOUT output is asserted. (The counter rolls over and keeps counting.)

In either case, when the TIN input is negated the ZDS status bit is zero, the TOUT output is negated, the counting stops, and the prescaler is forced to all ones (see Figure 5-5).



* Analog representation of counter value.

Figure 5-5. Device Watchdog Example

SECTION 6
ELECTRICAL SPECIFICATIONS

This section contains electrical specifications and associated timing information for the MC68230.

6.1 MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precuations be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

6.2 THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Rating
Thermal Resistance Ceramic Plastic	θ_{JA}	 50 TBD	°C/W

6.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts − Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins − User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

6.4 DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics		Symbol	Min	Max	Unit
Input High Voltage	All Inputs	V_{IH}	V_{SS} + 2.0	V_{CC}	V
Input Low Voltage	All Inputs	V_{IL}	V_{SS} − 0.3	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	H1, H3, R/$\overline{W}$, $\overline{RESET}$, CLK, RS1-RS5, $\overline{CS}$	I_{in}	–	10.0	μA
Hi-Z (Off State) Input Current (V_{in} = 0.4 to 2.4)	$\overline{DTACK}$, PC0-PC7, D0-D7 H2, H4, PA0-PA7, PB0-PB7	I_{TSI}	– −0.1	20 −1.0	μA mA
Output High Voltage (I_{Load} = −400 μA, V_{CC} = min) (I_{Load} = −150 μA, V_{CC} = min) (I_{Load} = −100 μA, V_{CC} = min)	$\overline{DTACK}$, D0-D7 H2, H4, PB0-PB7, PA0-PA7 PC0-PC7	V_{OH}	V_{SS} + 2.4	–	V
Output Low Voltage (I_{Load} = 8.8 mA, V_{CC} = min) (I_{Load} = 5.3 mA, V_{CC} = min) (I_{Load} = 2.4 mA, V_{CC} = min)	PC3/TOUT, PC5/$\overline{PIRQ}$ D0-D7, $\overline{DTACK}$ PA0-PA7, PB0-PB7, H2, H4, PC0-PC2, PC4, PC6, PC7	V_{OL}	–	0.5	V
Internal Power Dissipation (Measured at T_A = 0°C)		P_{INT}	–	750	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz)		C_{in}	–	15	pF

6.5 AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING (See Figure 6-1)

Characteristic	Symbol	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation	f	2.0	8.0	2.0	10.0	4.0	12.0	MHz
Cycle Time	t_{cyc}	125	500	100	500	80	250	ns
Clock Pulse Width	t_{CL} t_{CH}	55 55	250 250	45 45	250 250	35 35	125 125	ns
Clock Rise and Fall Times	t_{Cr} t_{Cf}	– –	10 10	– –	10 10	– –	5 5	ns

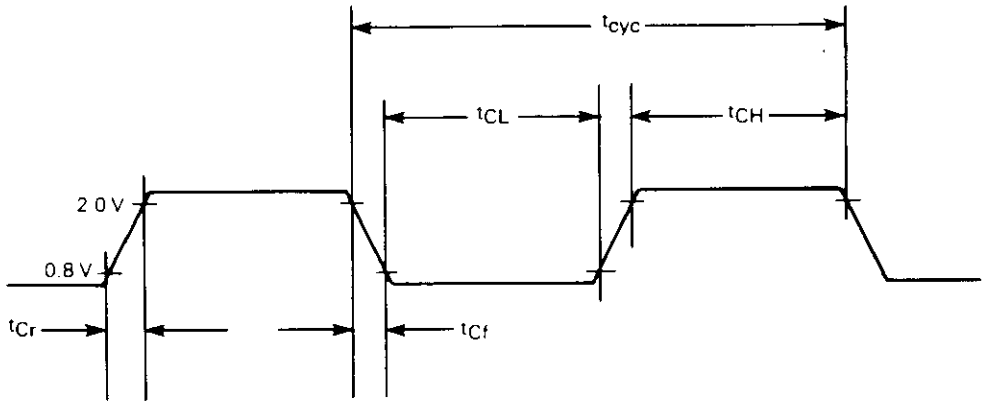


Figure 6-1. Clock Input Timing Diagram

6.6 AC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise noted)

Number	Characteristic	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
1	R/$\overline{W}$, RS1-RS5 Valid to CS Low (Setup Time)	0	–	0	–	0	–	ns
2(10)	$\overline{CS}$ Low to R/$\overline{W}$ and RS1-RS5 Invalid (Hold Time)	100	–	65	–	60	–	ns
3(1)	$\overline{CS}$ Low to CLK Low (Setup Time)	30	–	20	–	20	–	ns
4(2)	$\overline{CS}$ Low to Data Out Valid	–	75	–	60	–	55	ns
5	RS1-RS5 Valid to Data Out Valid	–	140	–	100	–	80	ns
6	CLK Low to $\overline{DTACK}$ Low (Read/Write Cycle)	0	70	0	60	0	55	ns
7(3)	$\overline{DTACK}$ Low to $\overline{CS}$ High (Hold Time)	0	–	0	–	0	–	ns
8	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to Data Out Invalid (Hold Time)	0	–	0	–	0	–	ns
9	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to D0-D7 High Impedance	–	50	–	45	–	45	ns
10	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to $\overline{DTACK}$ High	–	50	–	45	–	40	ns
11	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to $\overline{DTACK}$ High Impedance	–	100	–	55	–	45	ns
12	Data In Valid to $\overline{CS}$ Low (Setup Time)	0	–	0	–	0	–	ns
13	$\overline{CS}$ Low to Data In Invalid (Hold Time)	100	–	65	–	60	–	ns
14	Port Input Data Valid to H1(H3) Asserted (Setup Time)	100	–	60	–	50	–	ns
15	H1(H3) Asserted to Port Input Data Invalid (Hold Time)	20	–	20	–	20	–	ns
16	Handshake Input H1(H4) Pulse Width Asserted	40	–	40	–	40	–	ns
17	Handshake Input H1(H4) Pulse Width Negated	40	–	40	–	40	–	ns
18	H1(H3) Asserted to H2(H4) Negated (Delay Time)	–	150	–	120	–	100	ns
19	CLK Low to H2(H4) Asserted (Delay Time)	–	100	–	100	–	80	ns
20(4)	H2(H4) Asserted to H1(H3) Asserted	0	–	0	–	0	–	ns
21(5)	CLK Low to H2(H4) Pulse Negated (Delay Time)	–	125	–	125	–	100	ns
22(9,11)	Synchronized H1(H3) to CLK Low on which $\overline{DMAREQ}$ is Asserted	2.5	3.5	2.5	3.5	2.5	3.5	CLK Per.
23	CLK Low on which $\overline{DMAREQ}$ is Asserted to CLK Low on which $\overline{DMAREQ}$ is Negated	2.5	3	2.5	3	2.5	3	CLK Per.
24	CLK Low to Port Output Data Valid (Delay Time) (Modes 0 and 1)	–	150	–	120	–	100	ns
25(9,11)	Synchronized H1(H3) to Port Output Data Invalid (Modes 0 and 1)	1.5	2.5	1.5	2.5	1.5	2.5	CLK Per.
26	H1 Negated to Port Output Data Valid (Modes 2 and 3)	–	70	–	50	–	50	ns
27	H1 Asserted to Port Output Data High Impedance (Modes 2 and 3)	0	70	0	70	0	70	ns
28	Read Data Valid to $\overline{DTACK}$ Low (Setup Time)	0	–	0	–	0	–	ns
29	CLK Low to Data Output Valid, Interrupt Acknowledge Cycle	–	120	–	100	–	80	ns
30(7)	H1(H3) Asserted to CLK High (Setup Time)	50	–	40	–	40	–	ns
31	$\overline{PIACK}$ or $\overline{TIACK}$ Low to CLK Low (Setup Time)	50	–	40	–	30	–	ns
32(11)	Synchronized $\overline{CS}$ to CLK Low on which $\overline{DMAREQ}$ is Asserted	3	3	3	3	3	3	CLK Per.
33(9,11)	Synchronized H1(H3) to CLK Low on which H2(H4) is Asserted	3.5	4.5	3.5	4.5	3.5	4.5	CLK Per.
34	CLK Low to $\overline{DTACK}$ Low Interrupt Acknowledge Cycle (Delay Time)	–	100	–	100	–	80	ns
35	CLK Low to $\overline{DMAREQ}$ Low (Delay Time)	0	120	0	100	0	80	ns
36	CLK Low to $\overline{DMAREQ}$ High (Delay Time)	0	120	0	100	0	80	ns
37(11)	Synchronized H1(H3) to CLK Low on which $\overline{PIRQ}$ is Asserted	3	3	3	3	3	3	CLK Per.

6.6 AC ELECTRICAL SPECIFICATIONS (Continued)

Number	Characteristic	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
38(11)	Synchronized $\overline{CS}$ to CLK Low on which $\overline{PIRQ}$ is High Impedance	3	3	3	3	3	3	CLK Per.
39	CLK Low to PIRQ Low or High Impedance	0	250	0	225	0	200	ns
40(8)	TIN Frequency (External Clock) — Prescaler Used	0	1	0	1	0	1	f_{clk} (Hz) (6)
41	TIN Frequency (External Clock) — Prescaler Not Used	0	1/8	0	1/8	0	1/8	f_{clk} (Hz) (6)
42	TIN Pulse Width High or Low (External Clock)	55	—	45	—	45	—	ns
43	TIN Pulse Width Low (Run/Halt Control)	1	—	1	—	1	—	CLK Per.
44	CLK Low to TOUT High, Low, or High Impedance	0	250	0	225	0	200	ns
45	$\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ High to $\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ Low	50	—	30	—	30	—	ns

NOTES:

1. This specification only applies if the PI/T had completed all operations initiated by the previous bus cycle when $\overline{CS}$ was asserted. Following a normal read or write bus cycle, all operations are complete within three clocks after the falling edge of the CLK pin on which $\overline{DTACK}$ was asserted. If $\overline{CS}$ is asserted prior to completion of these operations, the new bus cycle, and hence, $\overline{DTACK}$ is postponed.

   If all operations of the previous bus cycle were complete when $\overline{CS}$ was asserted, this specification is made only to insure that $\overline{DTACK}$ is asserted with respect to the falling edge of the CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the $\overline{CS}$ setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later.

2. Assuming the RS1-RS5 to data valid time has also expired.

3. This specification imposes a lower bound on $\overline{CS}$ low time, guaranteeing that $\overline{CS}$ will be low for at least 1 CLK period.

4. This specification assures recognition of the asserted edge of H1(H3).

5. This specification applies only when a pulsed handshake option is chosen and the pulse is not shortened due to an early asserted edge of H1(H3).

6. CLK refers to the actual frequency of the CLK pin, not the maximum allowable CLK frequency.

7. If the setup time on the rising edge of the clock is not met, H1(H3) may not be recognized until the next rising of the clock.

8. This limit applies to the frequency of the signal at TIN compared to the frequency of the CLK signal during each clock cycle. If any period of the waveform at TIN is smaller than the period of the CLK signal at that instant, then it is likely that the timer circuit will completely ignore one cycle of the TIN signal.

   If these two signals are derived from different sources they will have different instantaneous frequency variations. In this case the frequency applied to the TIN pin must be distinctly less than the frequency at the CLK pin to avoid lost cycles of the TIN signal. With signals derived from different crystal oscillators applied to the TIN and CLK pins with fast rise and fall times, the TIN frequency can approach 80 to 90% of the frequency of the CLK signal without a loss of a cycle of the TIN signal.

   If these two signals are derived from the same frequency source then the frequency of the signal applied to TIN can be 100% of the frequency at the CLK pin. They may be generated by different buffers from the same signal or one may be an inverted version of the other. The TIN signal may be generated by an 'AND' function of the clock and a control signal.

9. The maximum value is caused by a peripheral access (H1(H3) asserted) and bus access ($\overline{CS}$ asserted) occurring at the same time.

10. See **1.4 BUS INTERFACE OPERATION** for exception.

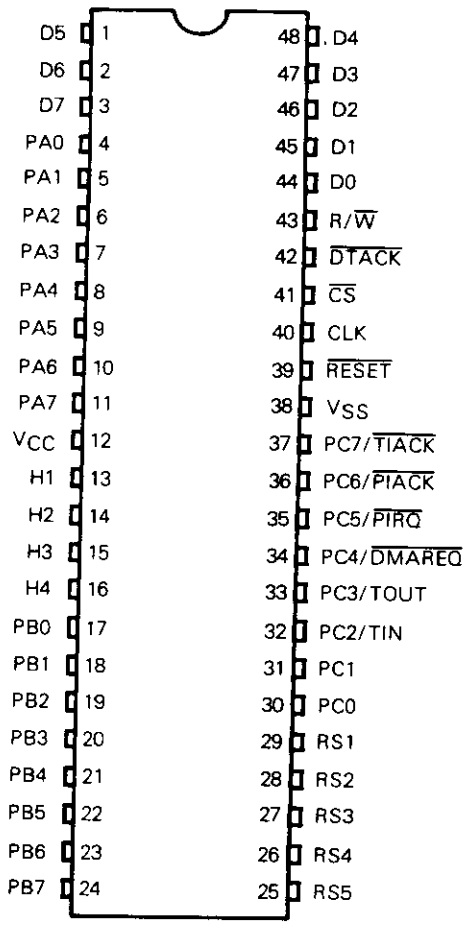
11. Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for $\overline{CS}$). (Refer to the **1.4 BUS INTERFACE OPERATION** for the exception concerning $\overline{CS}$.)

Timing diagrams (Figures 6-2, 6-3, 6-4, 6-5, and 6-6) are located on foldout pages 3, 4, 5, and 6 at the end of this document.

SECTION 7
MECHANICAL DATA AND ORDERING INFORMATION

This section contains the pin assignments and package dimensions of the MC68230. In addition, detailed information is provided to be used as a guide when ordering.

7.1 PIN ASSIGNMENT

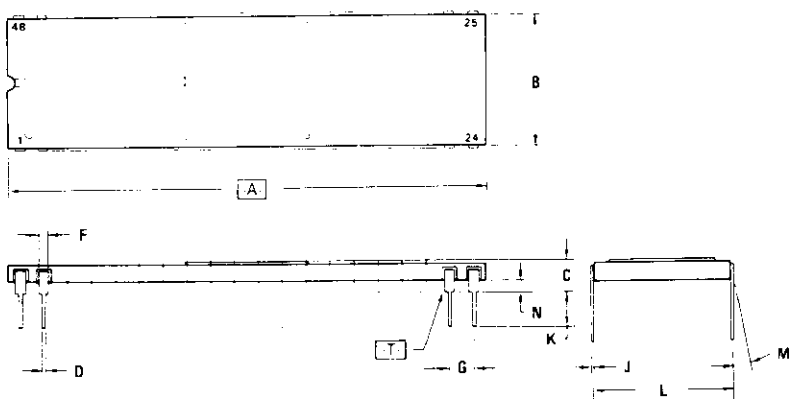


7.2 ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
Ceramic	8.0	0°C to 70°C	MC68230L8
L Suffix	10.0	0°C to 70°C	MC68230L10
	12.5	0°C to 70°C	MC68230L12
Plastic	8.0	0°C to 70°C	MC68230G8
G Suffix	10.0	0°C to 70°C	MC68230G10
	12.5	0°C to 70°C	MC68230G12

7.3 PACKAGE DIMENSIONS

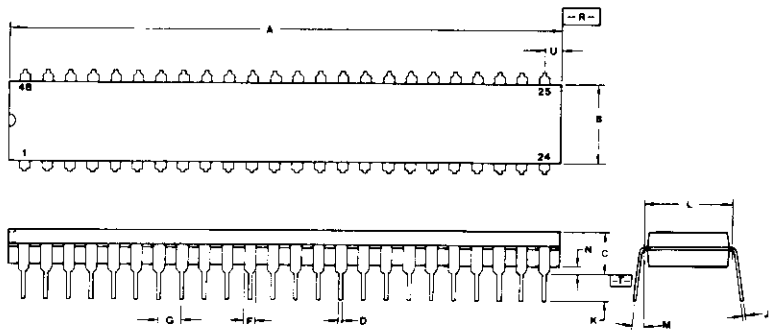
L SUFFIX
CERAMIC PACKAGE
CASE 740-02



NOTES:
1. DIMENSION A IS DATUM.
2. POSTIONAL TOLERANCE FOR LEADS: ⌖ Ø 0.25 (0.010) M T A M
3. T IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	60.35	61.57	2.376	2.424
B	14.63	15.34	0.576	0.604
C	3.05	4.32	0.120	0.160
D	0.381	0.533	0.015	0.021
F	0.762	1.397	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.203	0.330	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.65	0.590	0.616
M	0°	10°	0°	10°
N	1.016	1.524	0.040	0.060

G SUFFIX
PLASTIC PACKAGE
CASE 767-01



NOTES:
1. -R- IS END OF PACKAGE DATUM PLANE.
   -T- IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR LEADS 24 & 25:
   ⌖ 0.35 (0.014) T B Ⓜ R
   POSITIONAL TOLERANCE FOR LEAD PATTERN:
   ⌖ 0.25 (0.010) T B Ⓜ
3. DIM B DOES NOT INCLUDE MOLD FLASH.
4. DIM L IS TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	61.67	61.77	2.428	2.432
B	13.92	14.02	0.548	0.552
C	4.83	5.06	0.190	0.200
D	0.38	0.50	0.015	0.020
F	1.22	1.34	0.048	0.053
G	2.54 BSC		0.100 BSC	
J	0.25	0.30	0.010	0.012
K	3.23	3.37	0.127	0.133
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°
N	0.64	0.88	0.025	0.035
U	1.79 BSC		0.070 BSC	

Table 1-3. Register Model (Sheet 1 of 2)

Register Select Bits 5	4	3	2	1	7	6	5	4	3	2	1	0	Register Value After RESET (Hex Value)	
0	0	0	0	0	Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense	0 0	Port General Contol Register
0	0	0	0	1	*	SVCRQ Select		IPF Select		Port Interrupt Priority Control			0 0	Port Service Request Register
0	0	0	1	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port A Data Direction Register
0	0	0	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port B Data Direction Register
0	0	1	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port C Data Direction Register
0	0	1	0	1	Interrupt Vector Number						*	*	0 F	Port Interrupt Vector Register
0	0	1	1	0	Port A Submode		H2 Control			H2 Int Enable	H1 SVCRQ Enable	H1 Stat Ctrl	0 0	Port A Control Register
0	0	1	1	1	Port B Submode		H4 Control			H4 Int Enable	H3 SVCRQ Enable	H3 Stat Ctrl	0 0	Port B Control Register
0	1	0	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Port A Data Register
0	1	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Port B Data Register
0	1	0	1	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	***	Port A Alternate Register
0	1	0	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	***	Port B Alternate Register
0	1	1	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	****	Port C Data Register
0	1	1	0	1	H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S	****	Port Status Register
0	1	1	1	0	*	*	*	*	*	*	*	*	0 0	(Null)
0	1	1	1	1	*	*	*	*	*	*	*	*	0 0	(Null)

* Unused, read as zero
** Value before RESET
*** Current value on pins
**** Undetermined value

Table 1-3. Register Model (Sheet 2 of 2)

Register Select Bits 5	4	3	2	1	7	6	5	4	3	2	1	0	Register Value After RESET (Hex Value)	
1	0	0	0	0	TOUT/TIACK Control			Z D Ctrl	*	Clock Control		Timer Enable	0 0	Timer Control Register
1	0	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 F	Timer Interrupt Vector Register
1	0	0	1	0	*	*	*	*	*	*	*	*	0 0	(Null)
1	0	0	1	1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	* *	Counter Preload Register (High)
1	0	1	0	0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	* *	Counter Preload Register (Mid)
1	0	1	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	* *	Counter Preload Register (Low)
1	0	1	1	0	*	*	*	*	*	*	*	*	0 0	(Null)
1	0	1	1	1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	* *	Count Register (High)
1	1	0	0	0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	* *	Count Register (Mid)
1	1	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	* *	Count Register (Low)
1	1	0	1	0	*	*	*	*	*	*	*	ZDS	0 0	Timer Status Register
1	1	0	1	1	*	*	*	*	*	*	*	*	0 0	(Null)
1	1	1	0	0	*	*	*	*	*	*	*	*	0 0	(Null)
1	1	1	0	1	*	*	*	*	*	*	*	*	0 0	(Null)
1	1	1	1	0	*	*	*	*	*	*	*	*	0 0	(Null)
1	1	1	1	1	*	*	*	*	*	*	*	*	0 0	(Null)

*Unused, read as zero
**Value before RESET

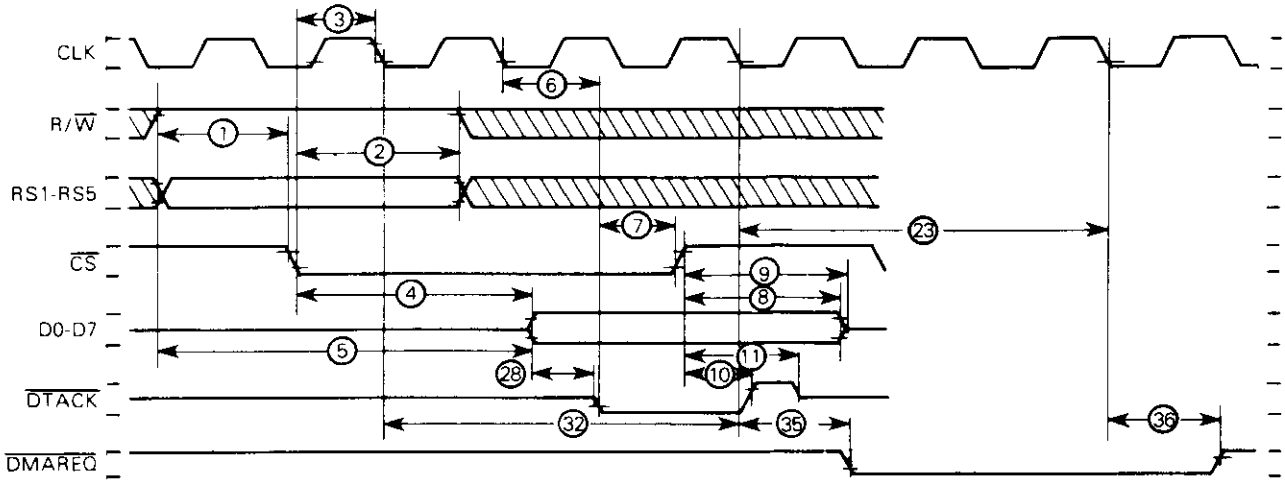


Figure 6-2. Read Cycle Timing Diagram

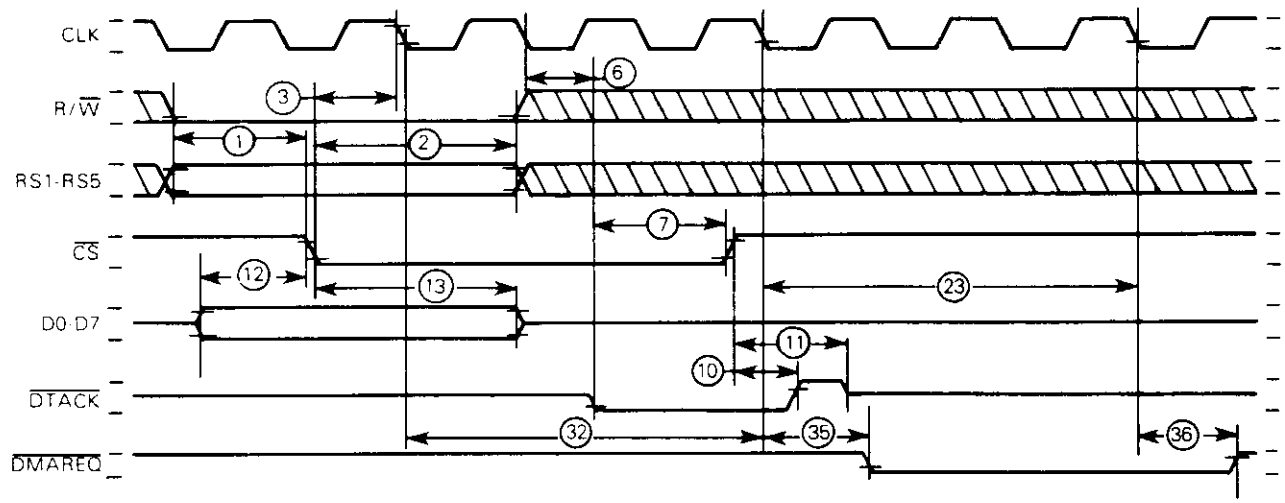
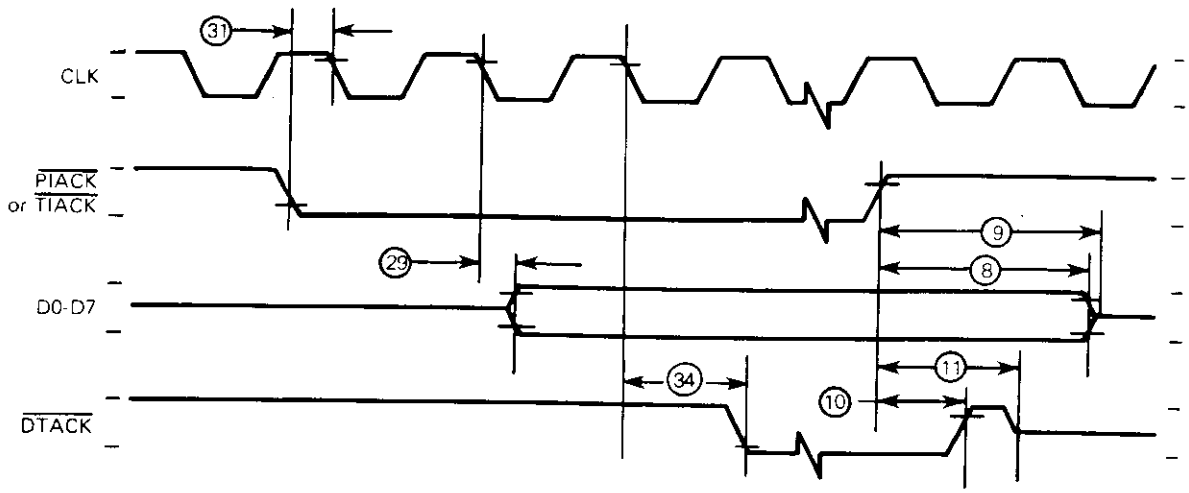


Figure 6-3. Write Cycle Timing Diagram

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

Figure 6-4. IACK Timing Diagram

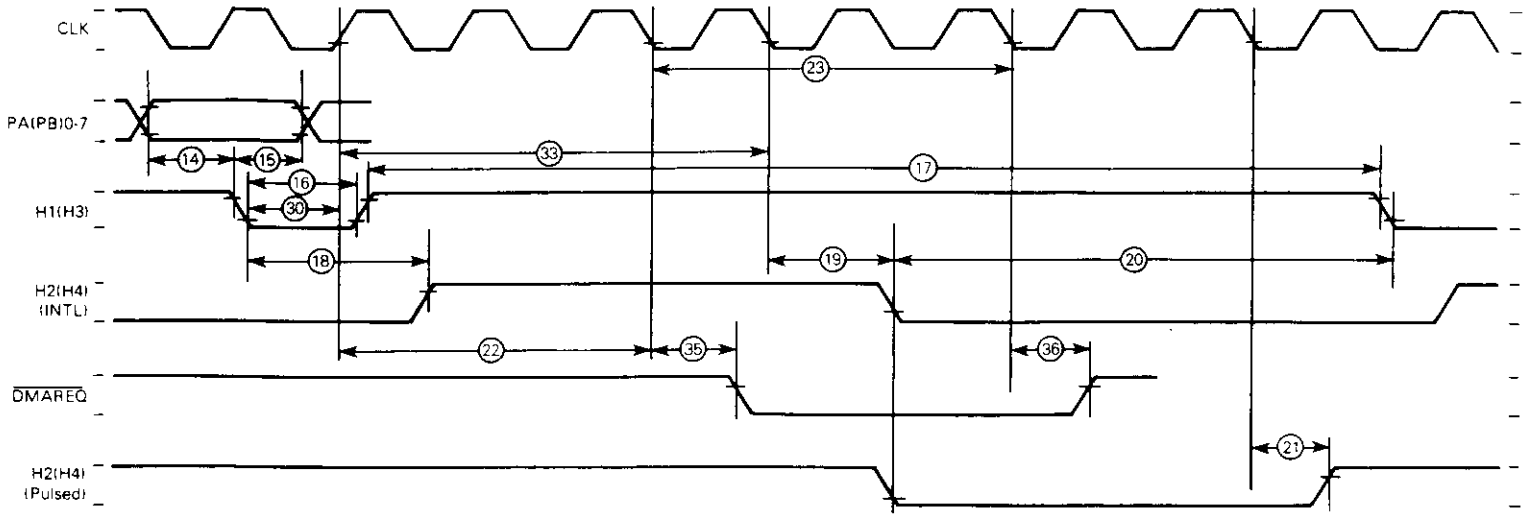


Figure 6-5. Peripheral Input Timing Diagram

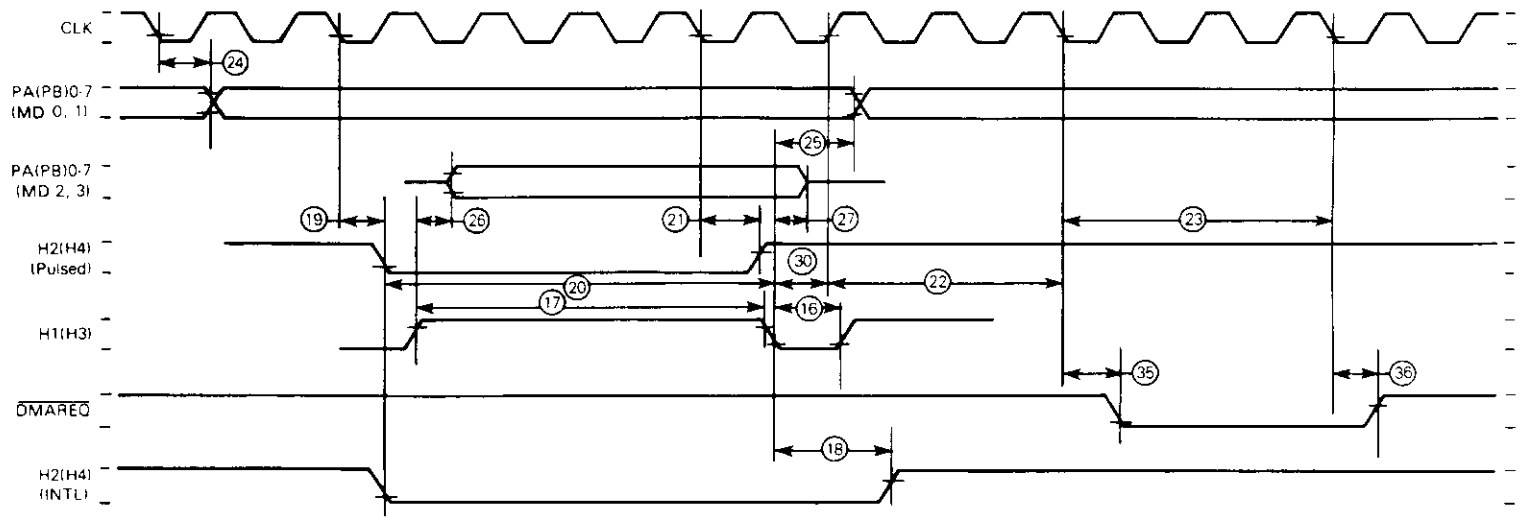


Figure 6-6. Peripheral Output Timing Diagram

NOTES:
1. Timing diagram shows H1, H2, H3, and H4 asserted low.
2. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

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