HEF40098B

Hex inverting buffer; 3-state

Rev. 8 — 21 November 2011 **Product data sheet**

1. General description

The HEF40098B is a hex inverting buffer with 3-state outputs. The 3-state outputs are controlled by two active LOW enable inputs (1$\overline{\text{OE}}$ and 2$\overline{\text{OE}}$). A HIGH on 1$\overline{\text{OE}}$ causes four of the six active LOW buffer elements (1$\overline{\text{Y}}$0 to 1$\overline{\text{Y}}$3) to assume a high-impedance or OFF-state regardless of the other input conditions and a HIGH on 2$\overline{\text{OE}}$ causes the outputs of the remaining two buffer elements (2$\overline{\text{Y}}$0 and 2$\overline{\text{Y}}$1) to assume a high-impedance or OFF-state regardless of the other input conditions.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from –40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

All types operate from –40 °C to +85 °C

Type number	Package		
	Name	Description	Version
HEF40098BP	DIP16	plastic dual in-line package; 16-leads (300 mil)	SOT38-4
HEF40098BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram

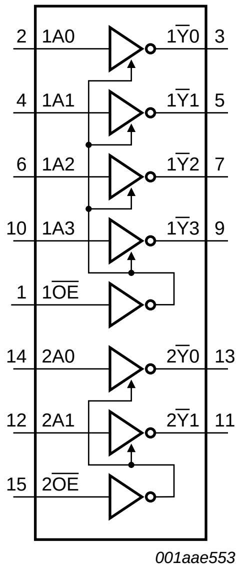


Fig 1. Functional diagram

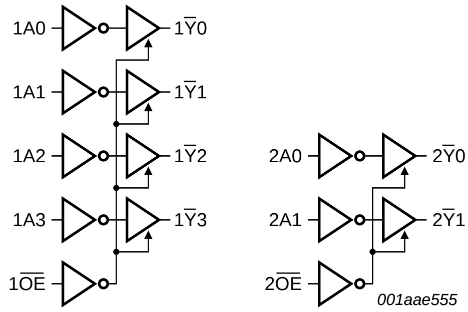


Fig 2. Logic diagram

5. Pinning information

5.1 Pinning

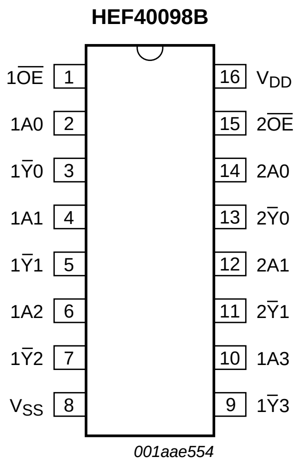


Fig 3. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{OE}$	1	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 10	buffer input
1$\overline{Y}$0, 1$\overline{Y}$1, 1$\overline{Y}$2, 1$\overline{Y}$3	3, 5, 7, 9	buffer output (active LOW)
V_{SS}	8	supply voltage
2$\overline{Y}$0, 2$\overline{Y}$1	13, 11	buffer output (active LOW)
2A0, 2A1	14, 12	buffer input
2$\overline{OE}$	15	output enable input (active LOW)
V_{DD}	16	supply voltage

6. Functional description

Table 3. Function table[1]

Inputs		Output
nAn	**n$\overline{OE}$**	**n$\overline{Y}$n**
H	L	L
L	L	H
X	H	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don’t care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+18	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{DD} + 0.5$ V		-	±10	mA
V_I	input voltage			–0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{DD} + 0.5$ V		-	±10	mA
$I_{I/O}$	input/output current			-	±10	mA
I_{DD}	supply current			-	50	mA
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
P_{tot}	total power dissipation	T_{amb} = –40 to +85 °C				
		DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation			-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	ns/V
		V_{DD} = 10 V	-	-	0.5	ns/V
		V_{DD} = 15 V	-	-	0.08	ns/V

9. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = –40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\lvert I_O \rvert$ < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\lvert I_O \rvert$ < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\lvert I_O \rvert$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\lvert I_O \rvert$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	–3.8	-	–3.2	-	–2.5	mA
		V_O = 4.6 V	5 V	-	–1.2	-	–1.0	-	–0.8	mA
		V_O = 9.5 V	10 V	-	–3.8	-	–3.2	-	–2.5	mA
		V_O = 13.5 V	15 V	-	–12.0	-	–10.0	-	–8.0	mA
I_{OL}	LOW-level output current	V_O = 0.4 V;	4.75 V	3.5	-	2.9	-	2.3	-	mA
		V_O = 0.5 V;	10 V	12.0	-	10.0	-	8.0	-	mA
		V_O = 1.5 V;	15 V	24.0	-	20.0	-	16.0	-	mA
I_I	input leakage current	V_I = 0 V or 15 V	15 V	-	0.3	-	0.3	-	1.0	μA
I_{DD}	supply current	I_O = 0 A	5 V	-	4	-	4	-	30	μA
			10 V	-	8	-	8	-	60	μA
			15 V	-	16	-	16	-	120	μA
I_{OZ}	OFF-state output current		15 V	-	1.6	-	1.6	-	12.0	μA
C_I	input capacitance			-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Figure 6; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nAn to n$\overline{Y}$n; see Figure 4	5 V	70 ns + (0.20 ns/pF)C_L	-	80	160	ns
			10 V	31 ns + (0.08 ns/pF)C_L	-	35	70	ns
			15 V	22 ns + (0.06 ns/pF)C_L	-	25	50	ns
t_{PLH}	LOW to HIGH propagation delay	nAn to n$\overline{Y}$n; see Figure 4	5 V	50 ns + (0.30 ns/pF)C_L	-	65	130	ns
			10 V	24 ns + (0.13 ns/pF)C_L	-	30	60	ns
			15 V	23 ns + (0.05 ns/pF)C_L	-	25	50	ns
t_{THL}	HIGH to LOW output transition time	see Figure 4	5 V	15 ns + (0.30 ns/pF)C_L	-	30	60	ns
			10 V	10 ns + (0.11 ns/pF)C_L	-	15	30	ns
			15 V	7 ns + (0.07 ns/pF)C_L	-	10	20	ns
t_{TLH}	LOW to HIGH output transition time	see Figure 4	5 V	10 ns + (0.50 ns/pF)C_L	-	35	70	ns
			10 V	8 ns + (0.24 ns/pF)C_L	-	20	40	ns
			15 V	6 ns + (0.18 ns/pF)C_L	-	15	30	ns
t_{PHZ}	HiGH to OFF-state propagation delay	n$\overline{OE}$, to n$\overline{Y}$n; see Figure 5	5 V		-	45	85	ns
			10 V		-	35	65	ns
			15 V		-	30	60	ns
t_{PLZ}	LOW to OFF-state propagation delay	n$\overline{OE}$, to n$\overline{Y}$n; see Figure 5	5 V		-	65	135	ns
			10 V		-	40	80	ns
			15 V		-	35	70	ns
t_{PZH}	OFF-state to HIGH propagation delay	n$\overline{OE}$, to n$\overline{Y}$n; see Figure 5	5 V		-	70	140	ns
			10 V		-	35	75	ns
			15 V		-	30	65	ns
t_{PZL}	OFF-state to LOW propagation delay	n$\overline{OE}$, to n$\overline{Y}$n; see Figure 5	5 V		-	90	185	ns
			10 V		-	40	85	ns
			15 V		-	35	70	ns

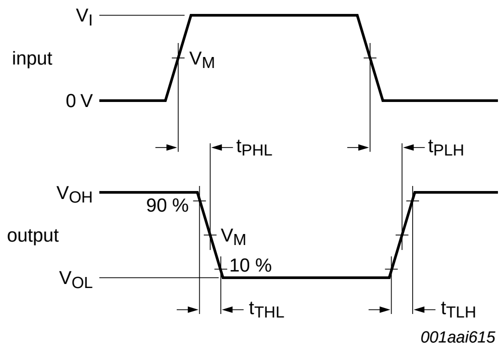
[1] The typical value of the propagation delay and transition times are calculated from the extrapolation formula as shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

P_D can be calculated (in μW) from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

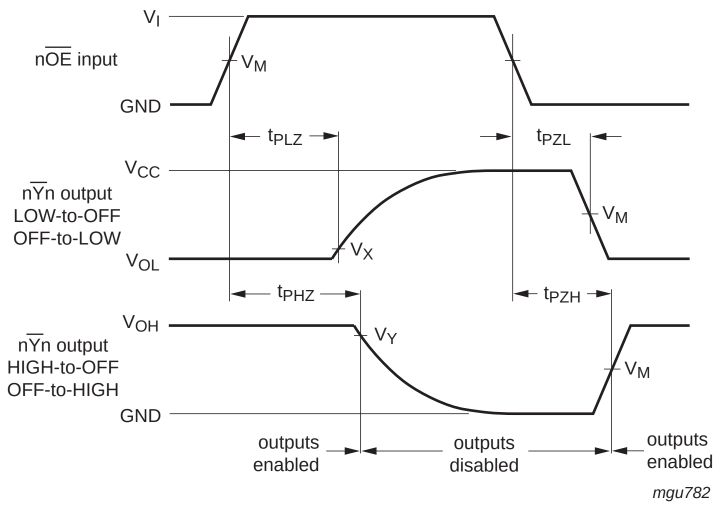
Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 5000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
		10 V	$P_D = 22800 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz,
		15 V	$P_D = 81000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF,
				V_{DD} = supply voltage in V,
				$\Sigma(C_L \times f_o)$ = sum of the outputs.

11. AC waveforms



Measurement points are given in Table 9, V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Input (nAn) to output ($n\overline{Y}n$) propagation delays

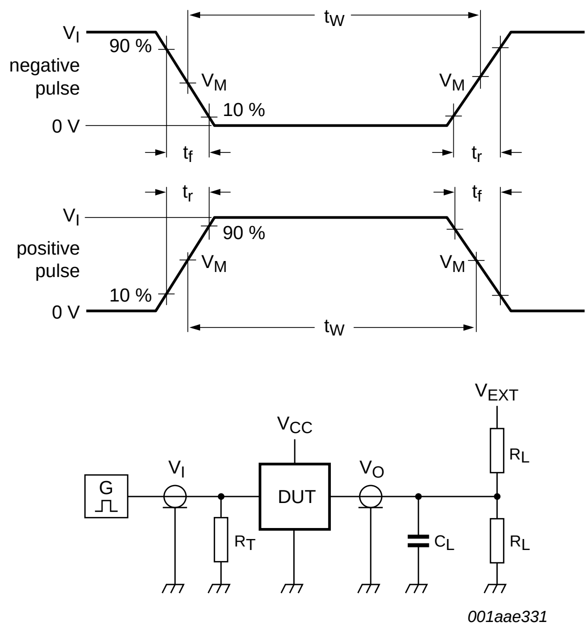


Measurement points are given in Table 9, V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. 3-state enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_{DD}$	$0.9V_{DD}$



Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test;

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

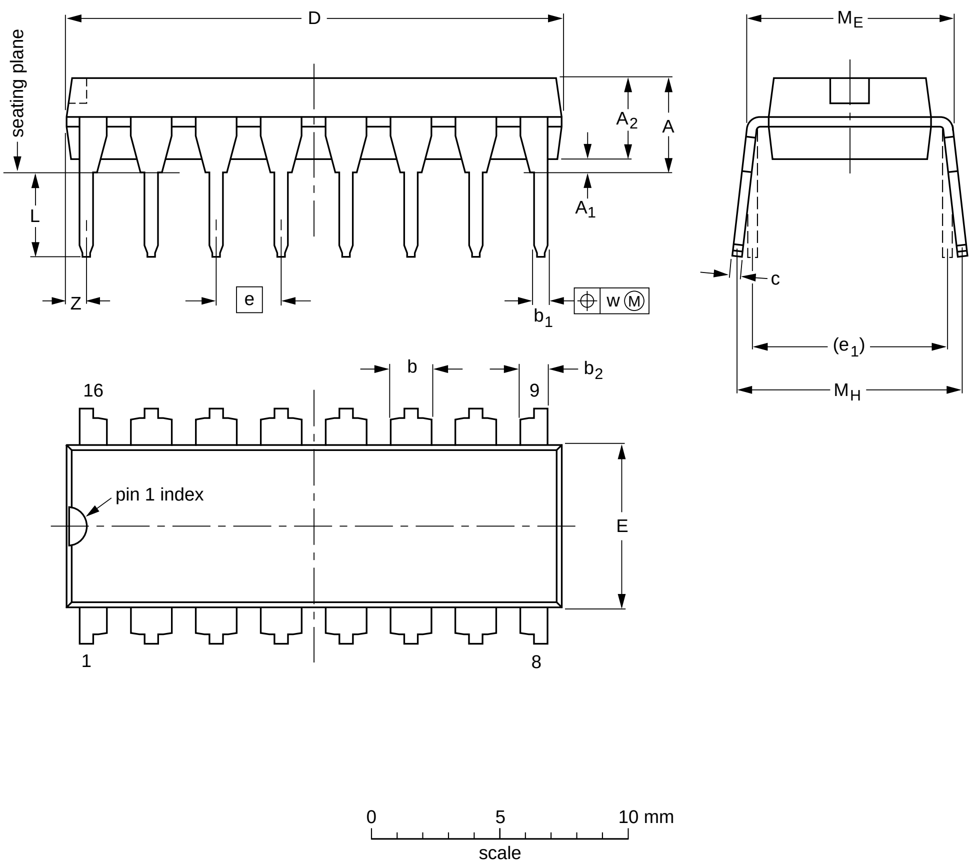
Fig 6. Test circuitry for switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
5 V to 15 V	V_{DD}	≤ 20 ns	50 pF	1 kΩ	open	$2V_{DD}$	GND

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D [(1)]	E [(1)]	e	e_1	L	M_E	M_H	w	Z [(1)] max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

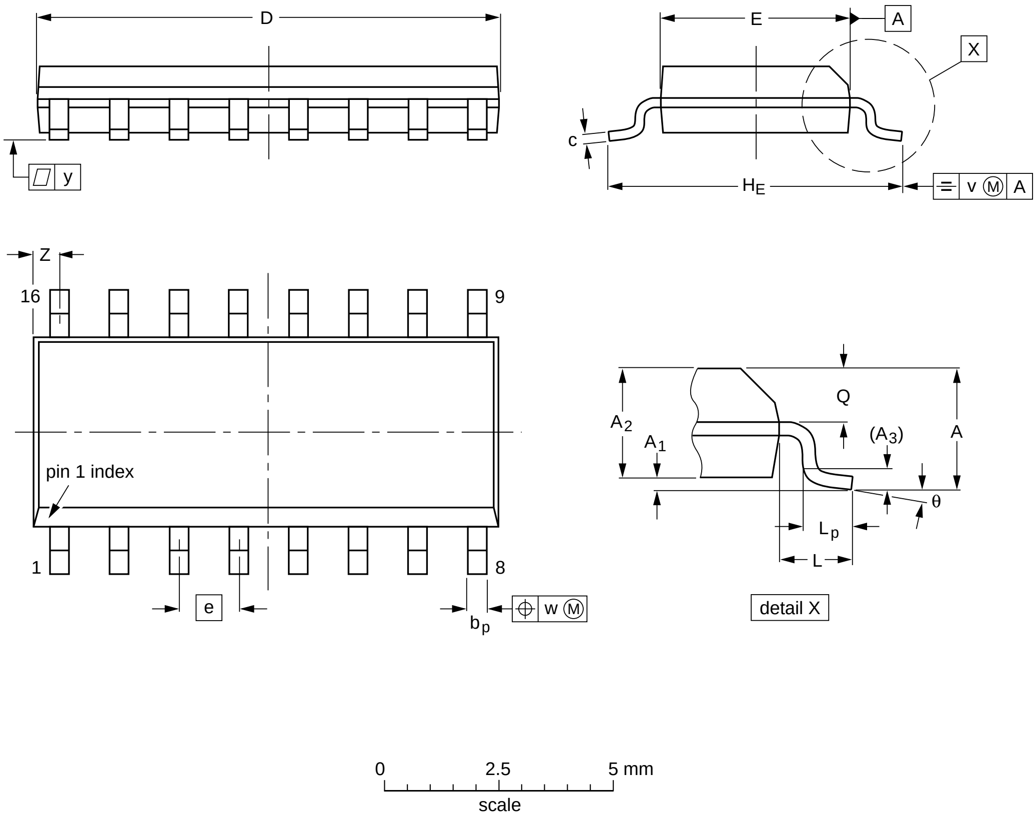
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 7. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT109-1 (SO16)

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF40098B v.8	20111121	Product data sheet	-	HEF40098B v.7
Modifications:	• Legal pages updated. • Changes in “General description” and “Features and benefits”. • Section “Applications” removed.			
HEF40098B v.7	20110914	Product data sheet	-	HEF40098B v.6
HEF40098B v.6	20090624	Product data sheet	-	HEF40098B v.5
HEF40098B v.5	20081031	Product data sheet	-	HEF40098B v.4
HEF40098B v.4	20080731	Product data sheet	-	HEF40098B_CNV v.3
HEF40098B_CNV v.3	19950101	Product specification	-	HEF40098B_CNV v.2
HEF40098B_CNV v.2	19950101	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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