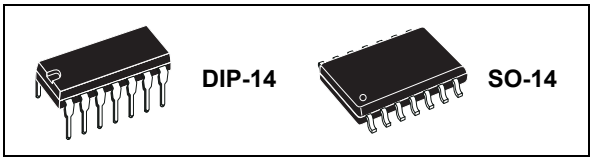
L6386E

High voltage high and low-side driver

Datasheet - production data



Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/nsec in full temperature range
- Driver current capability:
  - 400 mA source
  - 650 mA sink
- Switching times 50/30 nsec rise/fall with 1 nF load
- CMOS/TTL Schmitt trigger inputs with hysteresis and pull-down
- Undervoltage lockout on lower and upper driving section
- Integrated bootstrap diode
- Outputs in phase with inputs

Applications

- Home appliances
- Induction heating
- Industrial applications and drives
- Motor drivers
  - SR motors
  - DC, AC, PMDC and PMAC motors
- Asymmetrical half-bridge topologies
- HVAC
- Lighting applications
- Factory automation
- Power supply systems

Description

The L6386E is a high voltage gate driver, manufactured with the BCD™ "offline" technology, and able to drive simultaneously one high and one low-side power MOS or IGBT device. The high-side (floating) section is enabled to work with voltage rail up to 600 V. Both device outputs can independently sink and source 650 mA and 400 mA respectively and can be simultaneously driven high.

The L6386E device provides two input pins, two output pins and an enable pin (SD), and guarantees the outputs switch in phase with inputs. The logic inputs are CMOS/TTL compatible to ease the interfacing with controlling devices.

The L6386E integrates a comparator (inverting input internally referenced to 0.5 V) that can be used to protect the device against fault events, like the overcurrent. The DIAG output is a diagnostic pin, driven by the comparator, and used to signal a fault event occurrence to the controlling device.

The bootstrap diode is integrated in the driver allowing a more compact and reliable solution.

The L6386E device features the UVLO protection on both supply voltages (V_{CC} and V_{boot}) ensuring greater protection against voltage drops on the supply lines.

The device is available in a DIP-14 tube and SO-14 tube, and tape and reel packaging options.

Table 1. Device summary

Part number	Package	Packaging
L6386E	DIP-14	Tube
L6386ED	SO-14	Tube
L6386ED013TR		Tape and reel

This is information on a product in full production. www.st.com

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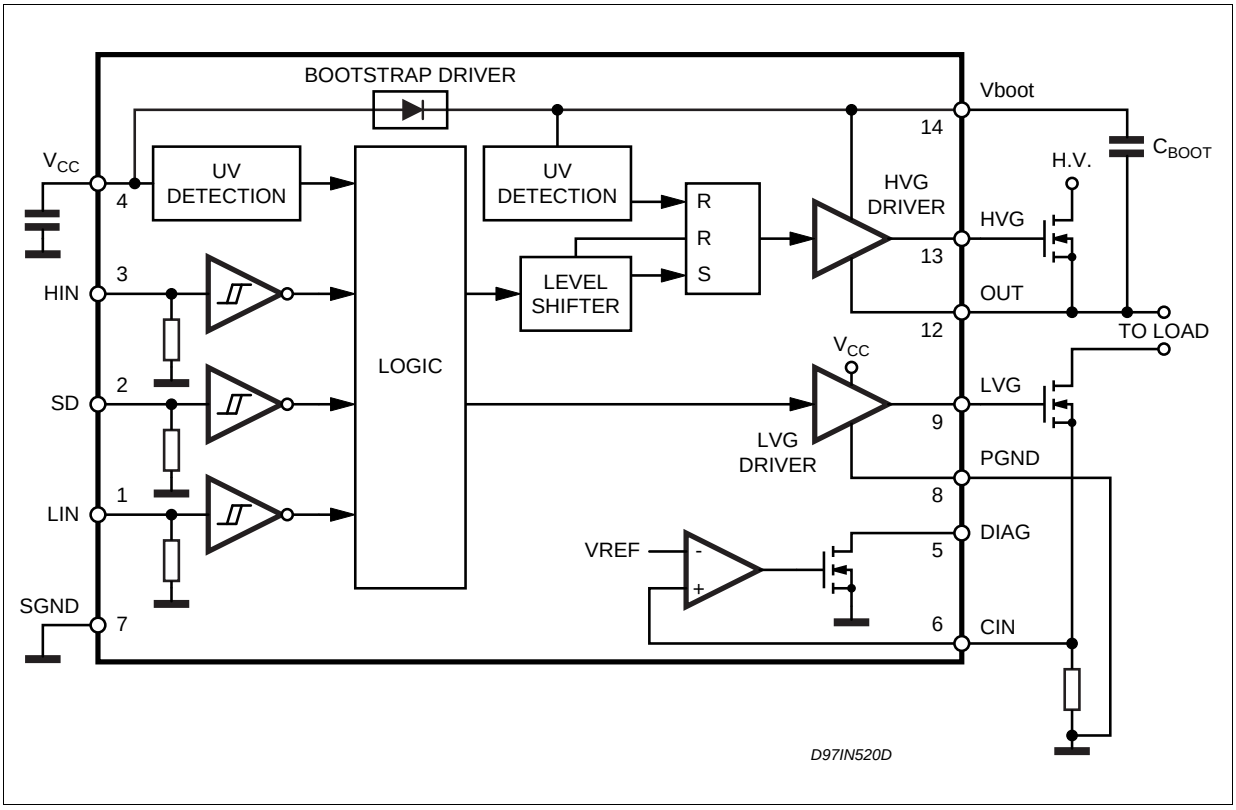
1 Block diagram

Figure 1. Block diagram



2 Electrical data

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{out}	Output voltage	-3 to V_{boot} - 18	V
V_{cc}	Supply voltage	- 0.3 to +18	V
V_{boot}	Floating supply voltage	-1 to 618	V
V_{hvg}	High-side gate output voltage	- 1 to V_{boot}	V
V_{lvg}	Low-side gate output voltage	-0.3 to V_{cc} +0.3	V
V_i	Logic input voltage	-0.3 to V_{cc} +0.3	V
V_{diag}	Open drain forced voltage	-0.3 to V_{cc} +0.3	V
V_{cin}	Comparator input voltage	-0.3 to V_{cc} +0.3	V
dV_{out}/dt	Allowed output slew rate	50	V/ns
P_{tot}	Total power dissipation (T_J = 85 °C)	750	mW
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-50 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	SO-14	DIP-14	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	165	100	°C/W

2.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{out}	12	Output voltage		(1)		580	V
V_{BS} (2)	14	Floating supply voltage		(1)		17	V
f_{sw}		Switching frequency	HVG, LVG load C_L = 1 nF			400	kHz
V_{cc}	4	Supply voltage				17	V
T_J		Junction temperature		-45		125	°C

1. If the condition V_{boot} - V_{out} < 18 V is guaranteed, V_{out} can range from -3 to 580 V.
2. V_{BS} = V_{boot} - V_{out}.

3 Pin connection

Figure 2.Pin connection (top view)

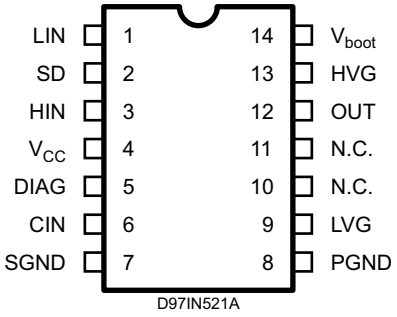


Table 5. Pin description

No.	Pin	Type	Function
1	LIN	I	Low-side driver logic input
2	SD(1)	I	Shutdown logic input
3	HIN	I	High-side driver logic input
4	V_{CC}	P	Low voltage supply
5	DIAG	O	Open drain diagnostic output
6	CIN	I	Comparator input
7	SGND	P	Ground
8	PGND	P	Power ground
9	LVG (1)	O	Low-side driver output
10, 11	N.C.		Not connected
12	OUT	P	High-side driver floating driver
13	HVG (1)	O	High-side driver output
14	V_{boot}	P	Bootstrapped supply voltage

1. The circuit guarantees 0.3 V maximum on the pin (at Isink = 10 mA), with V_{CC} > 3 V. This allows to omit the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver assures low impedance also in SD condition.

4 Electrical characteristics

4.1 AC operation

V_{CC} = 15 V; T_J = 25 °C

Table 6. AC operation electrical characteristics

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{on}	1, 3 vs. 9, 13	High/low-side driver turn-on propagation delay	V_{out} = 0 V		110	150	ns
t_{off}		High/low-side driver turn-off propagation delay			110	150	ns
t_{sd}	2 vs. 9, 13	Shut down to high/low-side propagation delay			105	150	
t_r	9, 13	Rise time	C_L = 1000 pF		50		ns
t_f		Fall time	C_L = 1000 pF		30		ns

4.2 DC operation

V_{CC} = 15 V; T_J = 25 °C

Table 7. DC operation electrical characteristics

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Low supply voltage section							
V_{ccth1}	4	V_{cc} UV turn-on threshold		11.5	12	12.5	V
V_{ccth2}		V_{cc} UV turn-off threshold		9.5	10	10.5	V
V_{cchys}		V_{cc} UV hysteresis			2		V
I_{qccu}		Undervoltage quiescent supply current	$V_{cc} \leq$ 11 V		200		µA
I_{qcc}		Quiescent current	V_{cc} = 15 V		250	320	µA
Bootstrapped supply section							
V_{boot}	14	Bootstrap supply voltage				17	V
V_{bth1}		V_{boot} UV turn-on threshold		10.7	11.9	12.9	V
V_{bth2}		V_{boot} UV turn-off threshold		8.8	9.9	10.7	V
V_{bhys}		V_{boot} UV hysteresis			2		V
I_{qboot}		V_{boot} quiescent current	HVG ON			200	µA
I_{lk}		High voltage leakage current	$V_{hvg} = V_{out} = V_{boot}$ = 600 V			10	µA
R_{dson}		Bootstrap driver on-resistance(1)	$V_{cc} \geq$ 12.5 V; V_{IN} = 0 V		125		Ω

Table 7. DC operation electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Driving buffers section							
I_{so}	9, 13	High/low-side source short-circuit current	$V_{IN} = V_{ih}$ (t_p < 10 µs)	300	400		mA
I_{si}	9, 13	High/low-side sink short-circuit current	$V_{IN} = V_{il}$ (tp < 10 µs)	500	650		mA
Logic inputs							
V_{il}	1,2,3	Low level logic threshold voltage				1.5	V
V_{ih}		High level logic threshold voltage		3.6			V
I_{ih}		High level logic input current	V_{IN} = 15 V		50	70	µA
I_{il}		Low level logic input current	V_{IN} = 0 V			1	µA
Sense comparator							
V_{io}		Input offset voltage		-10		10	mV
I_{io}	6	Input bias current	$V_{cin} \geq 0.5$		0.2		µA
V_{ol}	2	Open drain low level output voltage	I_{od} = -2.5 mA			0.8	V
V_{ref}		Comparator reference voltage		0.46	0.5	0.54	V

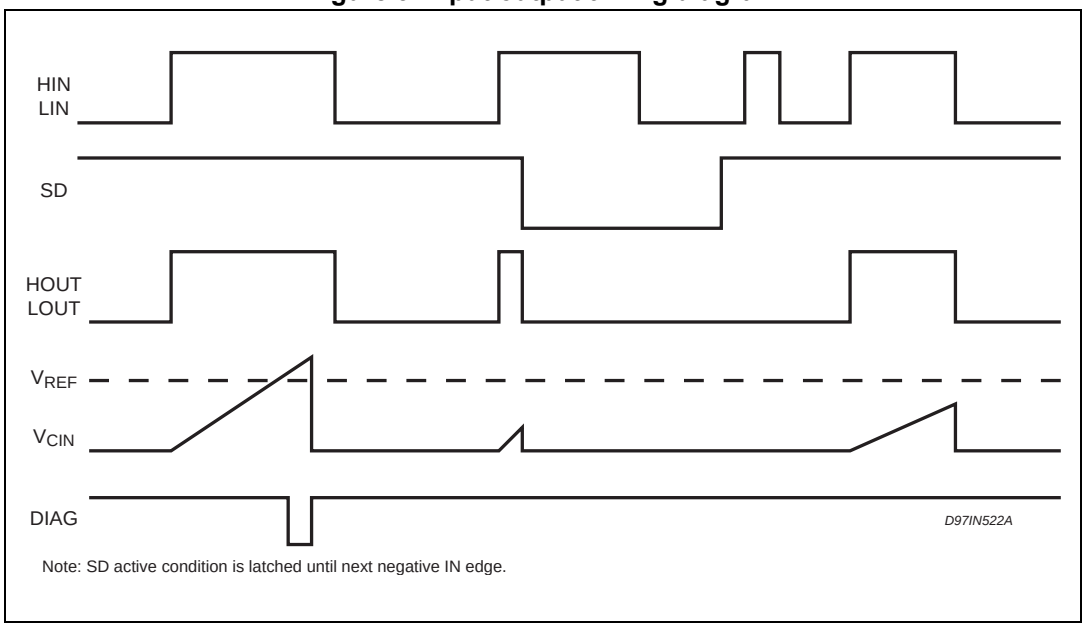
1. $R_{DS(on)}$ is tested in the following way:

$$R_{DSON} = \frac{(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})}{I_1(V_{CC}, V_{CBOOT1}) - I_2(V_{CC}, V_{CBOOT2})}$$

where I_1 is pin 14 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$.

4.3 Timing diagram

Figure 3. Input/output timing diagram



Note: SD active condition is latched until next negative IN edge.

5 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 4* a). In the L6386E device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 4* b. An internal charge pump (*Figure 4* b) provides the DMOS driving voltage. The diode connected in series to the DMOS has been added to avoid undesirable turn-on.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

$$C_{BOOT} >>> C_{EXT}$$

E.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage losses.

E.g.: HVG steady state consumption is lower than 200 µA, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply 1 µC to C_{EXT}. This charge on a 1 µF capacitor means a voltage drop of 1 V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSon} (typical value: 125 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 2

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q_{gate} is the gate charge of the external power MOS, R_{DSon} is the on-resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

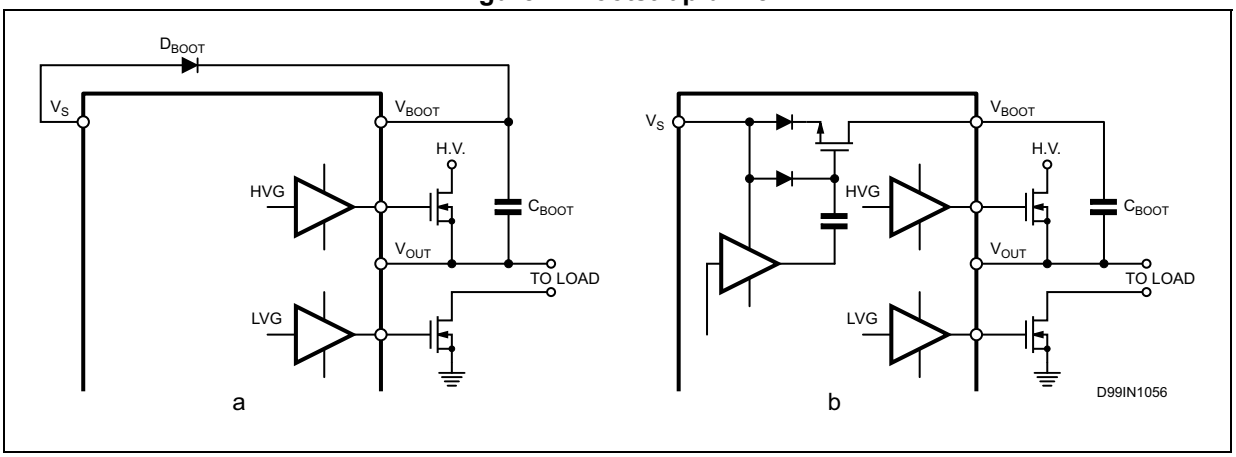
For example: using a power MOS with a total gate charge of 30 nC the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 µs. In fact:

Equation 3

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 4. Bootstrap driver



6 Typical characteristic

Figure 5. Typical rise and fall times vs. load capacitance

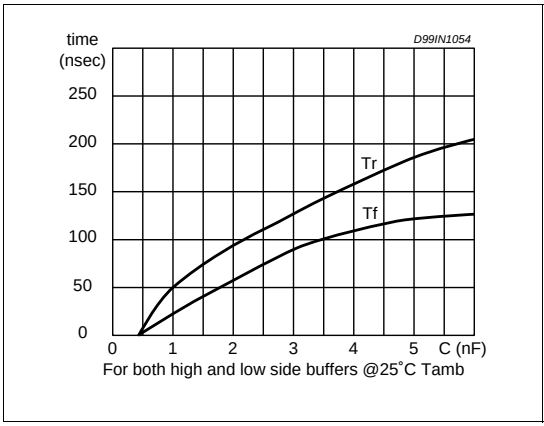


Figure 6. Quiescent current vs. supply voltage

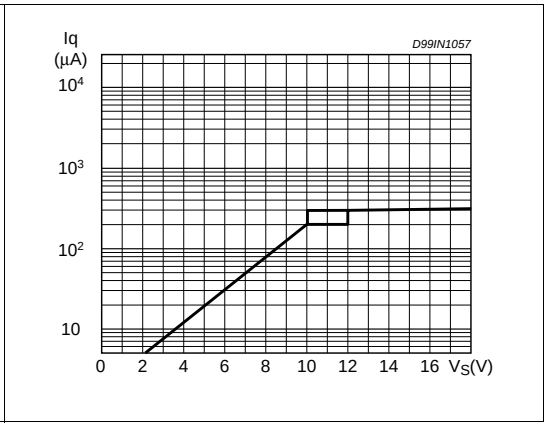


Figure 7. Turn-on time vs. temperature

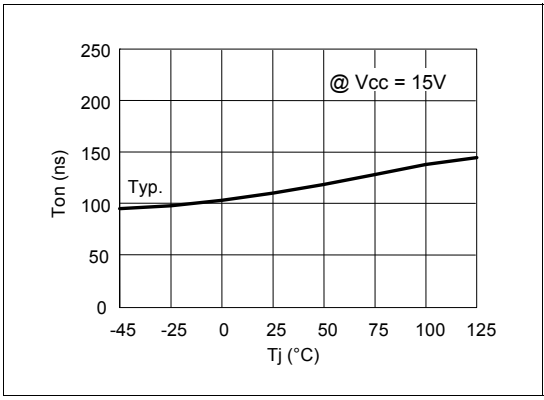


Figure 8. V_{BOOT} UV turn-on threshold vs. temperature

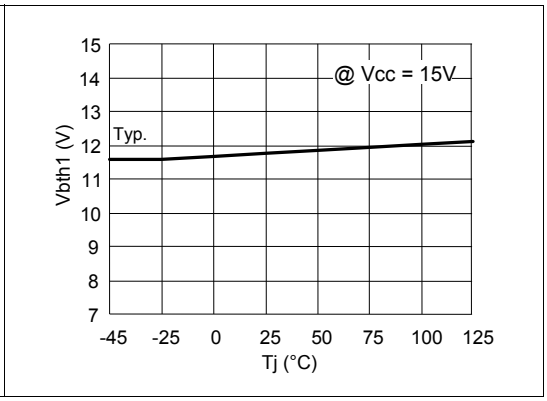


Figure 9. Turn-off time vs. temperature

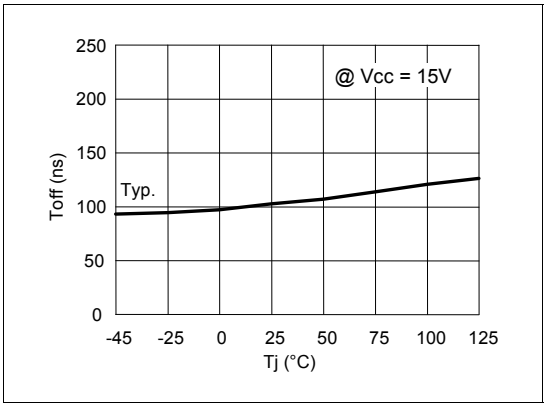


Figure 10. V_{BOOT} UV turn-off threshold vs. temperature

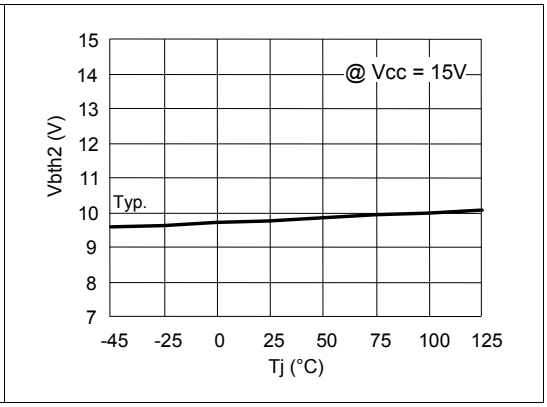


Figure 11. Shutdown time vs. temperature

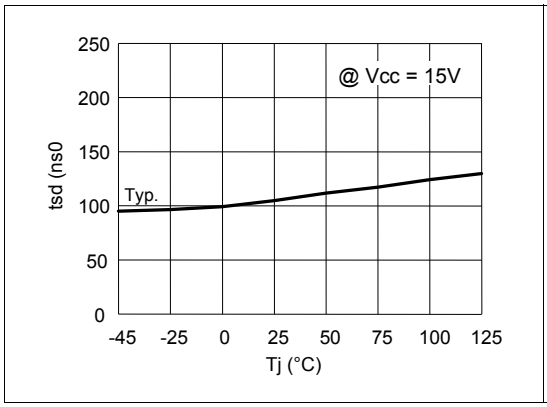


Figure 12. V_{BOOT} UV hysteresis

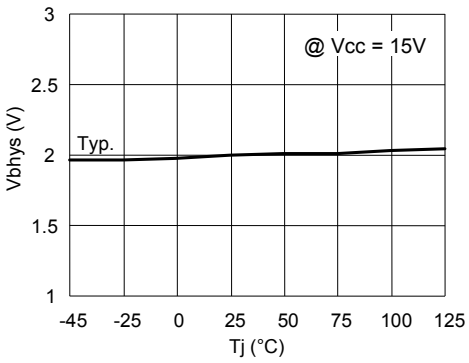


Figure 13. V_{CC} UV turn-on threshold vs. temperature

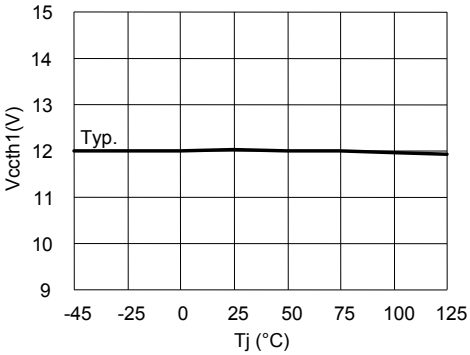


Figure 14. Output source current vs. temperature

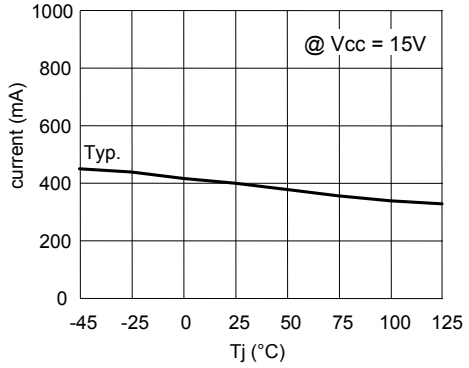


Figure 15. V_{CC} UV turn-off threshold vs. temperature

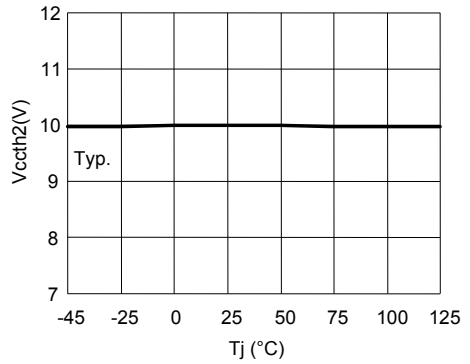


Figure 16. Output sink current vs. temperature

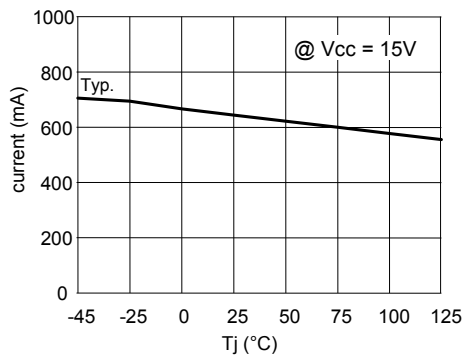
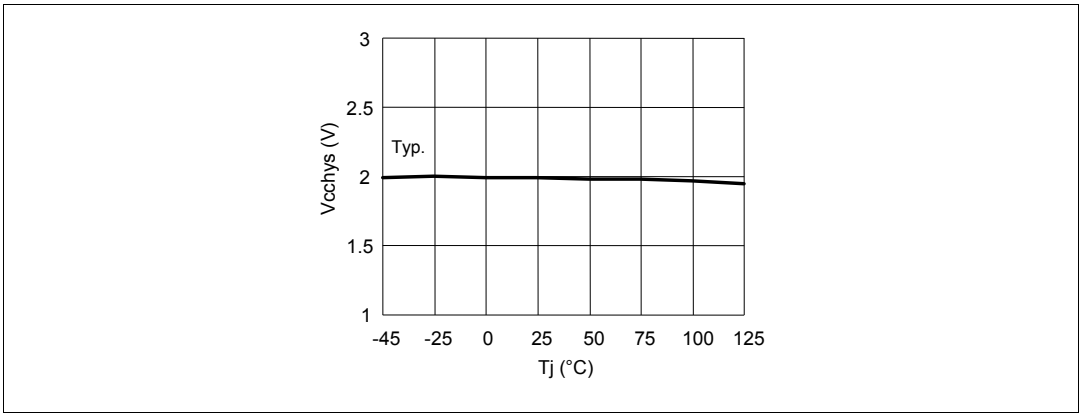


Figure 17. V_{CC} UV hysteresis vs. temperature



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 18. DIP-14 package outline

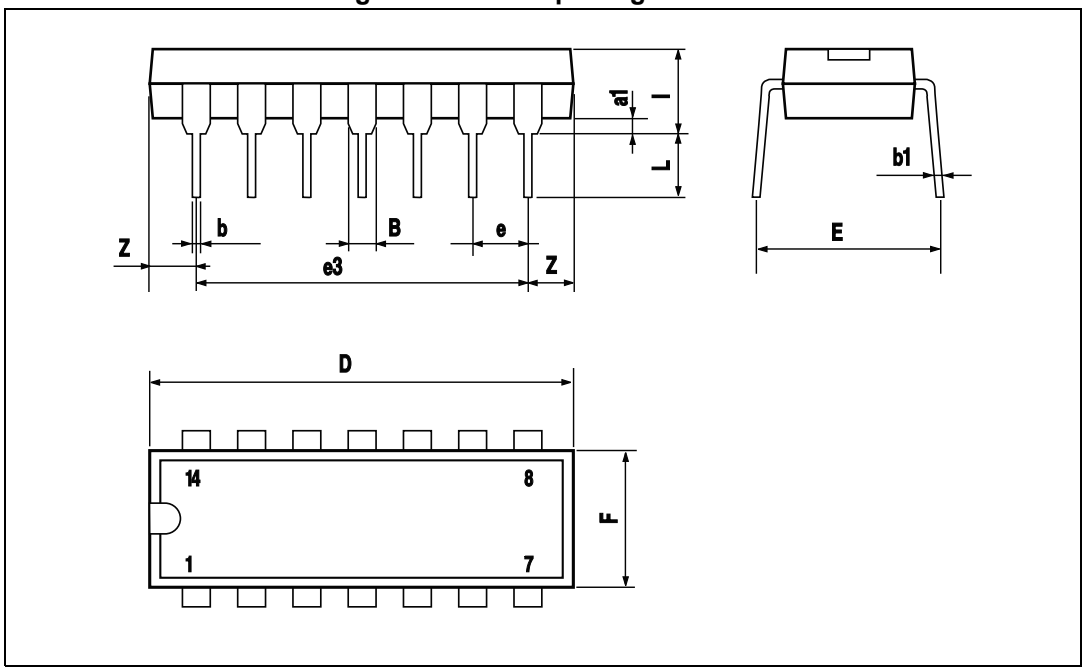


Table 8. DIP-14 package mechanical data

Symbol	Dimensions (mm)			Dimensions (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

Figure 19. SO-14 package outline

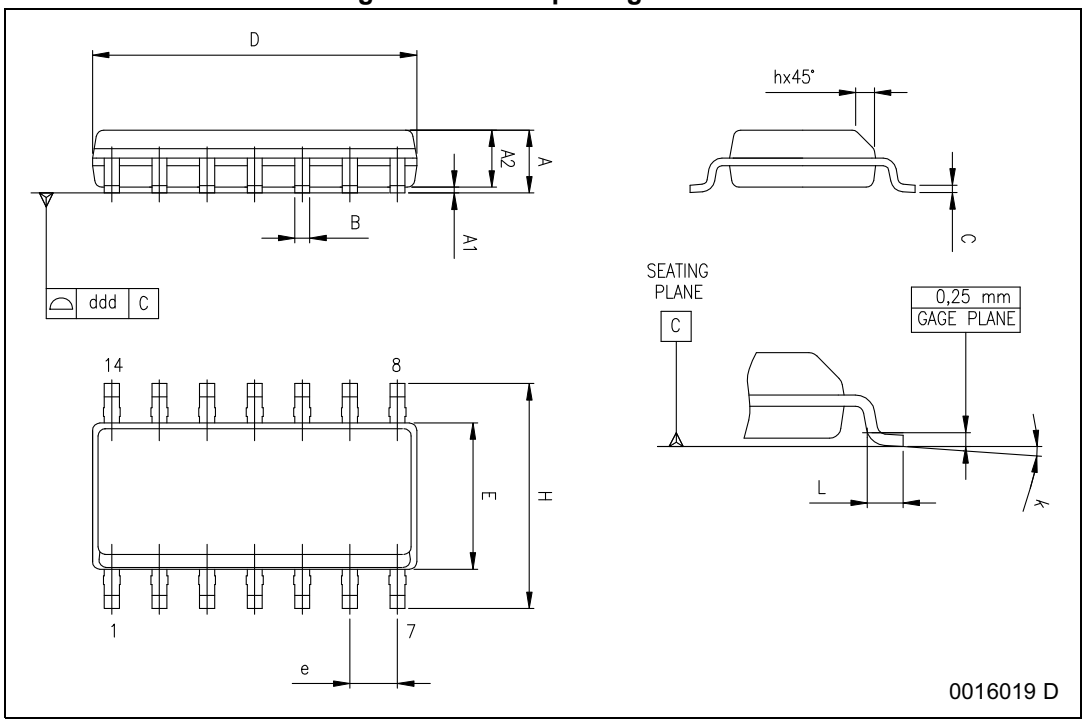


Table 9. SO-14 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.30	0.004		0.012
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.01
D(1)	8.55		8.75	0.337		0.344
E	3.80		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.20	0.228		0.244
h	0.25		0.50	0.01		0.02
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. “D” dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

8 Revision history

Table 10. Document revision history

Date	Revision	Changes
11-Oct-2007	1	First release
22-Jul-2009	2	Modified V_{bth2} on *Table 7*
20-Jun-2014	3	Added *Section : Applications on page 1*. Updated *Section : Description on page 1* (replaced by new description). Updated *Table 1: Device summary on page 1* (moved from page 17 to page 1, renamed title of *Table 1*). Updated *Figure 1: Block diagram on page 3* (moved from page 1 to page 3, added *Section 1: Block diagram on page 3*). Updated *Section 2.1: Absolute maximum ratings on page 4* (removed note below *Table 2: Absolute maximum ratings*). Updated *Table 5: Pin description on page 5* (updated “Type” of several pins). Updated *Table 7: DC operation electrical characteristics on page 6* (removed V_{CC} symbol including all parameters, test conditions and values). Numbered *Equation 1 on page 9*, *Equation 2 on page 9* and *Equation 3 on page 10*. Updated *Section 7: Package information on page 14* [updated/added titles, reversed order of *Figure 18* and *Table 8*, *Figure 19* and *Table 9* (numbered tables), removed 3D package figures, minor modifications]. Minor modifications throughout document.

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