

# M51397AP

SECAM CHROMA SYSTEM

## DESCRIPTION

The M51397AP is a semiconductor integrated circuit for SECAM system color television receivers. It CONTAINS chroma processor, chroma demodulator, DC regenerator and system switches for PAL/SECAM dual system. Dual system color television receivers can be implemented by M51395AP (PAL chroma system and video processor) and M51397AP (SECAM chroma processor and system switch).

## FEATURES

- Automatic mode switching for dual systems.
- Common delay line for dual systems.
- Minimum external components.
- Directly drives chroma output transistors.

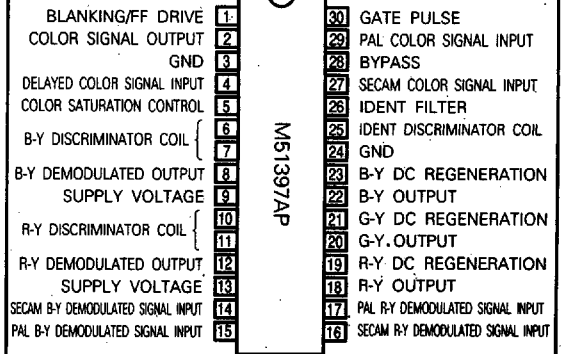
## APPLICATION

SECAM system color TV, color signal processors

## RECOMMENDED OPERATING CONDITION

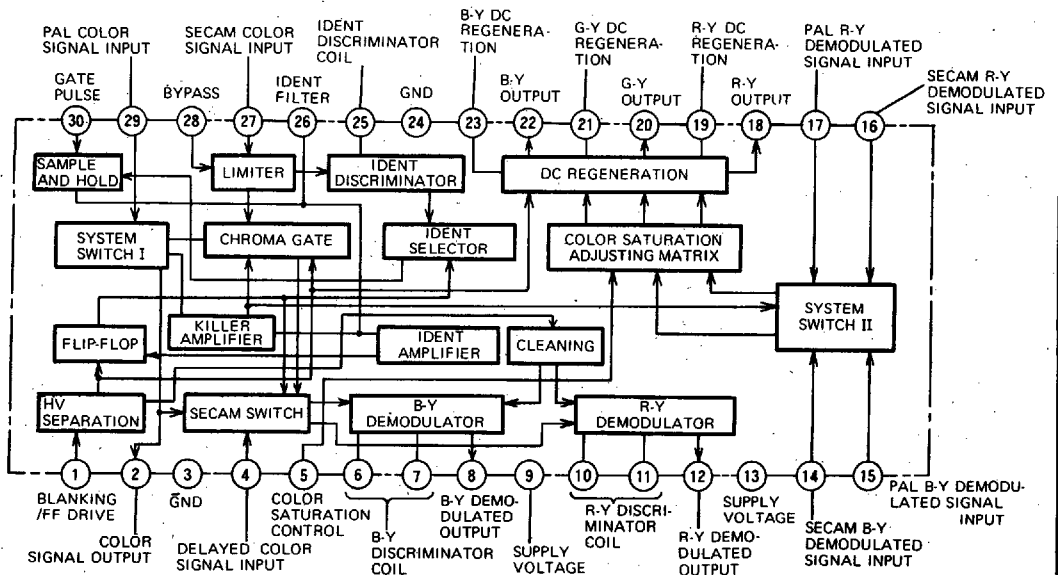
Supply voltage range.....11~13V  
 Rated supply voltage .....12V

## PIN CONFIGURATION (TOP VIEW)



Outline 30P4

## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Rated	Unit
V <sub>CC</sub>	Supply voltage	16.0	V
P <sub>d</sub>	Power dissipation	1400	mW
T <sub>opr</sub>	Operating temperature	-20~65	°C
T <sub>stg</sub>	Storage temperature	-40~125	°C

**ELECTRICAL CHARACTERISTICS** (T<sub>a</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Input signal	Conditions		Meas. point	Limits			Unit	Note	
			Input	V <sub>s</sub>		Min.	Typ.	Max.			
V <sub>CC</sub>	Supply voltage	SG1	27	6	9, 13	10	12	14	V	—	
I <sub>CC</sub>	Circuit current	SG1	27	6	a	55	75	88	mA	—	
V <sub>OLIM</sub>	Limiting output level	SG2	27	—	2	1.9	2.2	2.7	V <sub>P-P</sub>	1	
G <sub>LIM</sub>	Gain of limiter					28	32	36	dB	2	
V <sub>OSS</sub>	Output level of SECAM SW	SG1	27	—	6, 10	1.4	1.7	2.0	V <sub>P-P</sub>	—	
G <sub>SW</sub>	Gain of SECAM SW limiter	SG2	4	—		12	18	24	dB	3	
V <sub>ODIS</sub>	Output level of ident Disc.	SG2	27	—	25	0.48	0.59	0.70	V <sub>P-P</sub>	4	
V <sub>IK</sub>	Ident killer threshold level	SG1	27	6	20	38	48	58	dB	5	
V <sub>OK</sub>	Killed output level			8		18, 20, 22	—	5	20	mV <sub>P-P</sub>	6
E <sub>OB-Y</sub>	Demodulated output level	B-Y	SG1	27	—	b, c	0.86	0.98	1.13	V <sub>P-P</sub>	7
E <sub>OR-Y</sub>							R-Y	0.58	0.68		
$\frac{E_{OR-Y}}{E_{OB-Y}}$	Ratio of dem. output R-Y/B-Y	R-Y/B-Y	SG2	27	—	b, c	0.60	0.70	0.80	—	8
I <sub>lin I</sub>	Linearity of dem. output	I					27	—	2.4	2.8	3.2
I <sub>lin II</sub>		II	2.2	2.6	3.0	—	10				
ΔE <sub>OIH</sub>	Offset voltage of SECAM-SW	OFF	—	—	b, c	—	5	20	mV	10	
ΔE <sub>O/IN</sub>	Offset voltage vs input level	SG2	27	—	b, c	—	4	10	mV	11	
AMR	AMR	SG2	27	—		—	-30	-25	dB	12	
V <sub>COL</sub>	Color control voltage	OFF	—	—	5	5.6	6.0	6.4	V <sub>DC</sub>	13	
V <sub>SAT min</sub>	Color saturation control	MIN	SG1	27	5	18, 20, 22	—	—	-20	dB	14
V <sub>SAT grad</sub>		GRAD			5.78		-9.7	-5.7	-1.7		
V <sub>SAT max</sub>		MAX			7		1.6	4.1	6.6		
V <sub>SAT nor</sub>		NOR			5.88		2.8	4.0	5.6		
V <sub>OB-Y max</sub>	Maximum non distortion output voltage	B-Y	SG1	27	—	22	4.1	5.1	—	V <sub>P-P</sub>	15
V <sub>OR-Y max</sub>		R-Y				18	3.0	3.8	—		
V <sub>OG-Y max</sub>		G-Y				20	1.8	2.3	—		
V <sub>B-Y/R-Y</sub>	Output ratio of matrix	(B-Y)/(R-Y)	SG1	27	—	22, 18	115	130	145	%	16
V <sub>G-Y/R-Y</sub>						(G-Y)/(R-Y)	20, 18	52	60		
V <sub>18</sub>	Demodulated output DC voltage	SG1	27	4	18	6.6	7.2	7.8	V <sub>DC</sub>	17	
V <sub>20</sub>					20						
V <sub>22</sub>					22						
ΔV <sub>18-20</sub>	Offset voltage among output terminals	SG1	27	4	18	-0.1	0	0.1	V <sub>DC</sub>	18	
ΔV <sub>20-22</sub>					20						
ΔV <sub>22-18</sub>					22						
V <sub>CR B-Y</sub>	Cross talk of system SW (PAL-SECAM)	I	SG3	14, 16	6	22, 18	—	40	100	mV <sub>P-P</sub>	19
V <sub>CR R-Y</sub>		II		15, 17							
V <sub>OB-Y min</sub>	Output voltage at minimum color control	I	SG3	14, 16	4	18, 20, 22	—	20	50	mV <sub>P-P</sub>	20
V <sub>OR-Y min</sub>		II		15, 17							
E <sub>CR B-Y</sub>	Cross talk of demodulator	B-Y	SG1	27	8	22	33	38	—	dB	21
E <sub>CR R-Y</sub>		R-Y				18					



ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Input signal	Conditions		Meas. point	Limits			Unit	Note		
			Input	V <sub>s</sub>		Min.	Typ.	Max.				
V <sub>4</sub>	DC voltage at SECAM SW ④	I	OFF	—	—	4	2.2	2.8	3.4	V <sub>DC</sub>	22	
V <sub>4 min</sub>		II	—	—	—	—	0	0.5				
ΔE <sub>O I</sub>	Offset voltage of demodulated voltage between each H	I	SG1	27	—	b, c	—	10	20	mV <sub>DC</sub>	23	
ΔE <sub>O II</sub>		II	SG2	27, 4	—		—	20	50			
ΔV <sub>OR-Y/H</sub>	Offset voltage of output between each H		SG1	27	6		18	—	20	30	mV <sub>DC</sub>	24
ΔV <sub>OB-Y/H</sub>							22					
ΔV <sub>R-Y/COL</sub>	DC offset voltage vs color control		OFF	—	—		18	-30	0	30	mV <sub>DC</sub>	25
ΔV <sub>G-Y/COL</sub>							20					
ΔV <sub>B-Y/COL</sub>							22					
ΔV <sub>B-R/COL</sub>							18					
ΔV <sub>R-G/COL</sub>	DC offset voltage among outputs vs color control		OFF	—	—		20	-30	0	30	mV <sub>DC</sub>	26
ΔV <sub>G-B/COL</sub>							22					
ΔV <sub>O I</sub>							18					
V <sub>OR-YSII</sub>	Output voltage of system SW II/DC-clamp	I	SG3	14, 16	8		18	2.1	2.6	3.1	V <sub>P-P</sub>	27
V <sub>OB-YSII</sub>		II		15, 17			22					
V <sub>OS I</sub>	Output voltage of system SW I		SG2	29	—		2	1.5	1.9	2.3	V <sub>P-P</sub>	30
ΔE <sub>OCR I</sub>	Crosstalk of system SW I	I	SG2	27	—		2	—	40	100	mV <sub>P-P</sub>	31
ΔE <sub>OCR II</sub>		II		29			—	70	150			
ΔE <sub>OB-Y/V<sub>CC</sub></sub>	Change of demodulated output vs V		SG1	27	—		b	0.06	0.09	0.12	1/V	28
ΔE <sub>OR-Y/V<sub>CC</sub></sub>							c					
ΔE <sub>OB-Y/Ta</sub>	Change of demodulated output vs T		SG1	27	—		b	-2	0	2	mV/°C	29
ΔE <sub>OR-Y/Ta</sub>							c					
ΔV <sub>OR-Y/V<sub>CC</sub></sub>	Change of output voltage vs V		SG1	27	8		18	0.09	0.13	0.16	1/V	28
ΔV <sub>OG-Y/V<sub>CC</sub></sub>							20					
ΔV <sub>OB-Y/V<sub>CC</sub></sub>							22					
ΔV <sub>OR-Y/Ta</sub>	Change of output voltage vs T		SG1	27	8		18	-30	0	30	mV/°C	29
ΔV <sub>OG-Y/Ta</sub>							20					
ΔV <sub>OB-Y/Ta</sub>							22					
ΔV <sub>OB-R/V<sub>CC</sub></sub>	Offset voltage among output terminals vs V		OFF	—	—		18	-25	0	25	mV/V	32
ΔV <sub>OR-G/V<sub>CC</sub></sub>							20					
ΔV <sub>OG-B/V<sub>CC</sub></sub>							22					
ΔV <sub>OB-R/Ta</sub>	Offset voltage among output terminals vs T		OFF	—	—		18	-1	0	1	mV/°C	29
ΔV <sub>OR-G/Ta</sub>							20					
ΔV <sub>OG-B/Ta</sub>							22					

Symbol	Parameter	Meas. point	Limits			Unit	
			Min.	Typ.	Max.		
V <sub>G on</sub>	Gate pulse		30	1.4	—	—	V <sub>O-P</sub>
V <sub>G off</sub>				—	—	0.5	
V <sub>BLK on</sub>	Blanking pulse		1	6.8	—	—	V <sub>O-P</sub>
V <sub>BLK off</sub>				—	—	5.6	
V <sub>FF on</sub>	F.F. drive pulse		1	10.8	—	—	V <sub>O-P</sub>
V <sub>FF off</sub>				—	—	8.9	
V <sub>i max</sub>	Maximum chroma input signal at limiter		27	—	—	3.0	V <sub>P-P</sub>
V <sub>i dly</sub>	Input signal level at delayed input of SECAM SW		4	0.6	0.8	1.2	V <sub>P-P</sub>
V <sub>iSS max</sub>	Maximum input level of system SW		14-17	—	—	1.2	V <sub>P-P</sub>

## ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test terminal	Limits			Unit
			Min.	Typ.	Max.	
Ri (SEC)	SECAM Chroma input resistance	Pin 27	—	2.5	—	k $\Omega$
Ci (SEC)	SECAM Chroma input capacitance	Pin 27	—	1.6	—	pF
Ri (PAL)	PAL Chroma input resistance	Pin 29	—	3.0	—	k $\Omega$
Ro (C)	Chroma output resistance	Pin 2 R <sub>L</sub> =1.2k $\Omega$	—	20	—	$\Omega$
Ri (SW)	SECAM Switch input resistance	Pin 4	—	2.0	—	k $\Omega$
Cl (SW)	SECAM Switch input capacitance	Pin 4	—	3.5	—	pF
Ro (DISC)	SECAM SW Output impedance	Pins 6, 10	—	200	—	$\Omega$
Ri (DISC)	Discriminator input resistance	Pins 7, 11	—	1.8	—	k $\Omega$
Cl (DISC)	Discriminator input capacitance	Pins 7, 11	—	3.0	—	pF
Ro (DISC)	Discriminator output resistance	Pins 8, 12	—	300	—	$\Omega$
Ri (SYS)	System switch input resistance	Pins 14, 15, 16, 17	—	4.0	—	k $\Omega$
Ro (REG)	Demodulator output resistance	Pins 18, 20, 22	—	300	—	$\Omega$

## ELECTRICAL CHARACTERISTICS TEST METHOD

Note:1 V<sub>0</sub> (@SW3 → ON. Input signal  
f=4.3MHz, V<sub>0</sub>=100mV<sub>P-P</sub>)

Note:2 20log (V<sub>0</sub>-1/V<sub>0</sub>-2), where V<sub>0</sub>-1 (100mV<sub>P-P</sub>)  
→ V<sub>0</sub>-2 (@V<sub>0</sub> → 0), f=4.3MHz

Note:3 Same as Note 2 (input V<sub>0</sub>-1, 1V<sub>P-P</sub>, f=4.3MHz)

Note:4 Input signal f=4.328MHz, 200mV<sub>P-P</sub>

Note:5 20log (V<sub>0</sub>-1/V<sub>0</sub>-2) where V<sub>0</sub>-1 (100mV<sub>P-P</sub>)  
→ V<sub>0</sub>-2 (@V<sub>0</sub> → 0)

Note:6 Measured after eliminating SYNC pulses.

Note:7 Center Value of carrier @SW<sub>2</sub> → b, c

Note:8 V<sub>b</sub>/V<sub>c</sub>

Note:9 Output linearity (I) =  $\frac{(V_0 \text{ at } f_0 + 300\text{kHz}) - (V_0 \text{ at } f_0)}{(V_0 \text{ at } f_0 + 100\text{kHz}) - (V_0 \text{ at } f_0)}$

Output linearity (II) =  $\frac{(V_0 \text{ at } f_0 - 300\text{kHz}) - (V_0 \text{ at } f_0)}{(V_0 \text{ at } f_0 - 100\text{kHz}) - (V_0 \text{ at } f_0)}$

SW<sub>2</sub> → d, e, SW<sub>3</sub> → ON, 2200pF at b, c

Reference Signal at b: 4.406MHz (f<sub>OR</sub>), 200mV<sub>P-P</sub>

Reference Signal at c: 4.25MHz (f<sub>OS</sub>), 200mV<sub>P-P</sub>

Note:10 V<sub>0</sub> at 1H, (SW<sub>2</sub> → d, e, SW<sub>3</sub> → ON, SW<sub>4</sub> → ON,  
SW<sub>5</sub> → ON)

Note:11  $\Delta V_0$  at 20dB change of input signal

SW<sub>2</sub> → d, e, SW<sub>3</sub> → ON, SW<sub>4</sub> → ON, SW<sub>5</sub> → ON

Reference signal at b: 4.406MHz, 200mV<sub>P-P</sub>

Reference signal at c: 4.25MHz, 200mV<sub>P-P</sub>

DC Voltage between blanking interval and signal interval are adjusted to same voltage by L<sub>1</sub>, L<sub>2</sub>.

Note:12 20log VA/VF (db)

SW<sub>2</sub> → d, e, SW<sub>3</sub> → ON, Input signal voltage 200mV<sub>P-P</sub> without SYNC

Output voltage VF: SG2 4.25MHz, 4.406MHz FM modulated by fm=400Hz, 75kHz

Output voltage VA: SG2 4.25MHz, 4.406MHz AM modulated by fm=400Hz, 30%

Note:13 V<sub>0</sub> at No Load.

Note:14  $\frac{V_0 \text{ at } V_0}{V_0 \text{ at } V_0 = 6V}$  (dB) (SW<sub>2</sub> → b, c, SW<sub>6</sub> → k, l)

Note:15 Maximum Output Voltage without distortion at a change of V<sub>0</sub>

Note:16  $\frac{V_0 \text{ (B-Y)} - V_0 \text{ (G-Y)}}{V_0 \text{ (R-Y)} - V_0 \text{ (R-Y)}}$  (V<sub>0</sub> (R-Y)=2V<sub>P-P</sub>)

Note:17 DC voltage at V<sub>0</sub>=4V

Note:18 V<sub>0</sub>-V<sub>0</sub>, V<sub>0</sub>-V<sub>0</sub>, V<sub>0</sub>-V<sub>0</sub> (at V<sub>0</sub>=4V)

Note:19 SG3=0.4V<sub>P-P</sub>, 500kHz V<sub>0</sub>=6V SW<sub>2</sub>→d, e

I (Crosstalk SECAM → PAL)

Each output level at SW<sub>5</sub>→ON, SW<sub>6</sub>→k, l

II (Crosstalk PAL → SECAM)

Each output level at SW<sub>3</sub>→ON, SW<sub>5</sub>→OFF, SW<sub>6</sub>→m, n

Note:20 Same measurement as Note:23 at V<sub>0</sub> = 4V

Note:21 Ratio of output voltage between each line (dB), at SW<sub>2</sub> → d, e, SW<sub>4</sub> → ON

Note:22 I V<sub>0</sub> DC at SW<sub>3</sub> → ON

II V<sub>0</sub> DC at SW<sub>5</sub> → ON

Note:23 I Difference of output level between each line at SW<sub>2</sub> → d, e

II Difference of output level between each line at SW<sub>1</sub> → 2 SW<sub>2</sub> → d, e, V<sub>0</sub> → 1V<sub>P-P</sub>

Frequency at pin 27 and 4 are same (4.25 and 4.406MHz)

V<sub>0</sub> 1V<sub>P-P</sub>+3dB ~ 1V<sub>P-P</sub>-3dB

Note:24 Difference of output level between each line at SW<sub>2</sub> → b, c, SW<sub>6</sub> → k, l

Note:25 Difference of DC output voltage between as the change of color control

Note:26 Difference of DC output voltage between each output as the change of color control

Note:27 Output level at SG 0.4 V<sub>P-P</sub>, 500kHz, SW<sub>2</sub> de, color VR max

I SW3 → ON, SW6 → k, I  
 II SW3 → OFF, SW6 → m, n

Note:28  $V_{04} - V_{04}/4 - V_{04}$

where  $V_{04}$ ,  $V_{04}$ ,  $V_{04}$  are output voltages at supply voltage 10, 12, 14V.

Note:29 Topg-20 ~ +65°C.

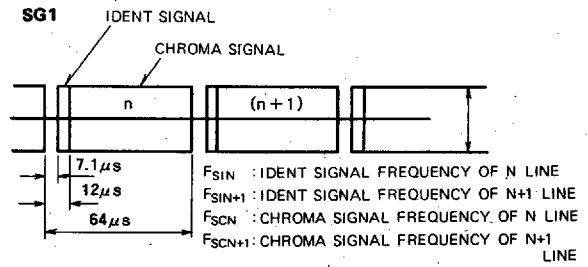
Note:30 Output level (after eliminating SYNC pulse) at input Signal 2  $V_{PP}$ .  $f=4.3\text{MHz}$

Note:31 I (Crosstalk SECAM → PAL) Input Signal at ②  
 100mV<sub>PP</sub>,  $f=4.3\text{MHz}$ , without SYNC pulse

II (Crosstalk PAL → SECAM) Input Signal at ③  
 2V<sub>PP</sub>,  $f=4.3\text{MHz}$ , SW3 → ON, SW5 → ON without SYNC pulse

Note:32 Change of output voltage via supply voltage 10, 12, 14 volts (mV/V).

INPUT SIGNAL



REFERENCE LEVEL 0dB :  $e_c = 100\text{mV}_{PP}$

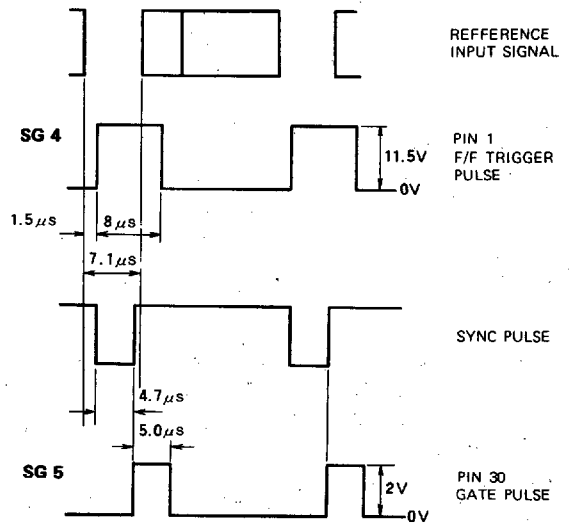
FREQUENCY OF SG1

Symbol	n line	n+1 line
$f_{s1}$	4.250	4.406
$f_{sc}$	$W = f_0$	4.250
	Y	4.020
	CY	4.3276
	G	4.0976
	MG	4.4024
	R	4.1724
	B	4.480
	BK	4.250

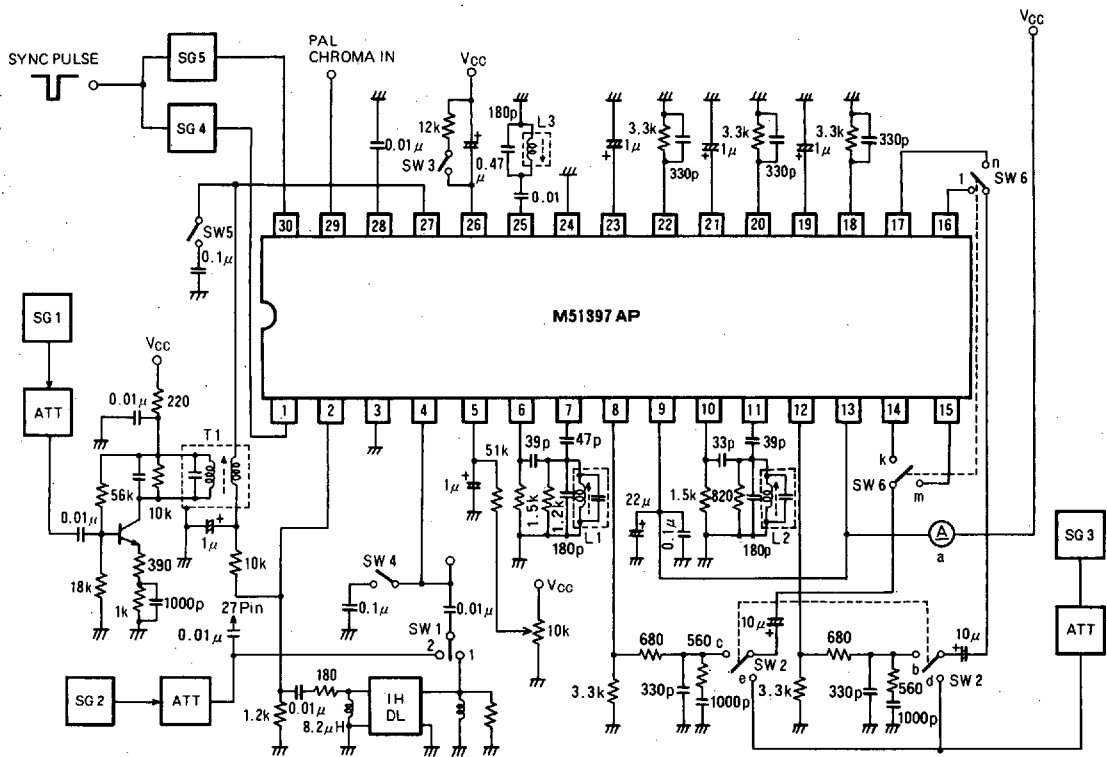
SG2 4.3 ± 0.5 MHz SINE WAVE

SG3 100K ~ 2 MHz SINE WAVE

Gate Pulse & F/F Trg. Pulse



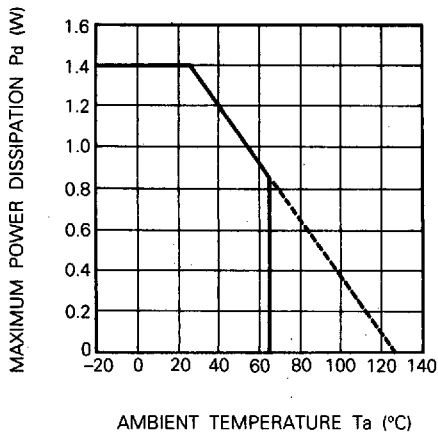
TEST CIRCUIT



Units Resistance:  $\Omega$   
Capacitance: F

TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)

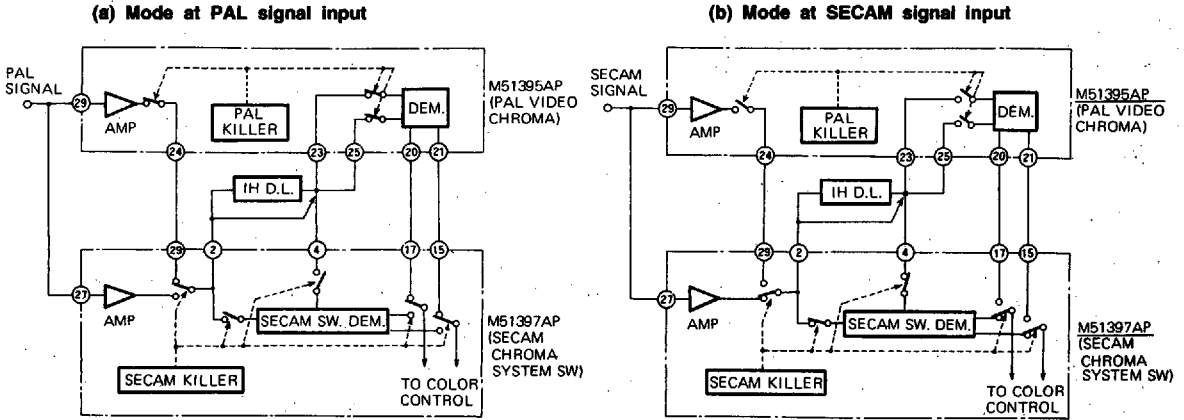


# M51397AP

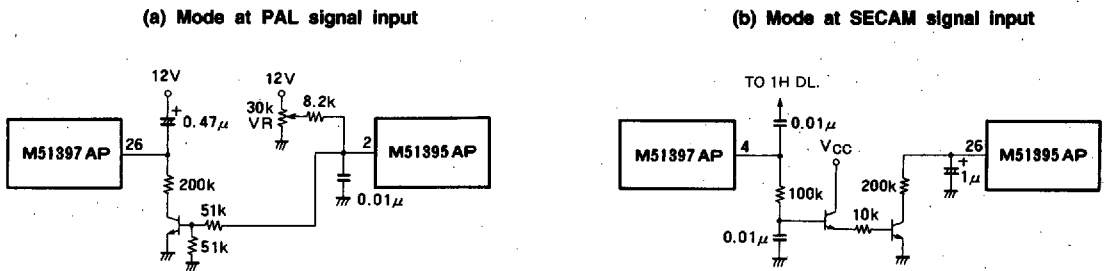
## SECAM CHROMA SYSTEM

### APPLICATION EXAMPLE OF M51395AP, M51397AP FOR PAL SECAM DUAL SYSTEM

#### MODE OF SYSTEM SW



### APPLICATION EXAMPLE FOR CONTROL OF THE PRIORITY OF THE DUAL MODE



### M51395AP (When the M51395AP is applied for PAL and SECAM dual system color TV)

Parts	Specification
Coil For D.L. CCT	<p>① ~ ② 16 Turns ② ~ ③ 16 Turns ④ ~ ⑤ 16 Turns ⑤ ~ ⑥ 16 Turns</p> <p>Bobbin: 10K type Pot Core: CT-31 Screw Core: C-2 Wire: 0.09φ 2UEW no load Q: 40</p>
Burst Cleaning and CW Phase Shift	<p>① ~ ③ 18 Turns</p> <p>Capacitor: 82PF RH type</p> <p>Bobbin: 10K type Pot Core: CT-31 Screw Core: C-2 Wire: 0.09φ 2UEW no load Q: 56</p>
D.L.	Type No. ADL-CS11 mfd by ASAHI GLASS CORP. JAPAN
X'tal	Type no. A9M2 mfd by Kinsekisha, Japan Load C: 16pF

M51397AP

Parts	Specification	
Bell Filter		<p>① - ③ 32 Turns ④ - ⑥ 8 Turns Capacitor : 82PF RH type</p> <p>Bobbin : 10K type Pot Core : CT-31 Screw Core : C-2 Wire : 0.1φ 2UEW no load Q : 36</p>
Ident Coil		<p>① - ③ 10 Turns with 2 wires (parallel)</p> <p>Bobbin : 10K type Pot Core : CT-31 Screw Core : C-2 Wire : 0.1φ 2UEW no load Q : 59</p>
Demo Coil		<p>① - ③ 18 Turns</p> <p>Capacitor : 82PF RH type</p> <p>Bobbin : 10K type Pot Core : CT-31 Screw Core : C-2 Wire : 0.1φ 2UEW no load Q : 55</p>
D.L.	The D.L. of M51395AP is applied commonly.	

A pot core and a screw core are manufactured by Taiyo Yuden, Japan.

**Adjustment of electrical characteristic for PAL/SECAM dual system circuit M51395AP/M51397AP.**

Adjustment is achieved as following sequence.

1. Bell filter transformer "T<sub>1</sub>" (M51397AP)  
Apply SECAM color signal to the input.  
Adjust bell filter transformer "T<sub>1</sub>" to make the color signal envelope at test point "TP<sub>2</sub>" into flat.
2. Ident discriminator coil "L<sub>1</sub>" (M51397AP)  
Adjust ident discriminator coil "L<sub>1</sub>" to give maximum ident filter voltage value at test point "TP<sub>1</sub>".
3. Discriminator (Demodulator) coil "T<sub>3</sub>/T<sub>4</sub>" (M51397AP)  
Adjust discriminator coil "T<sub>3</sub>/T<sub>4</sub>" to make the voltage of no color signal equal to the clamp voltage (~7.2V) at pins 18 and 22.
4. 4.433619MHz free run frequency (M51395AP)  
Apply PAL B/W signal (no burst) to input, and connect 0.01μF between pin 1 and GND.

Connect high input impedance frequency counter at pin 17.

Adjust the trimmer capacitor "C<sub>t</sub>" to frequency 4.433619MHz.

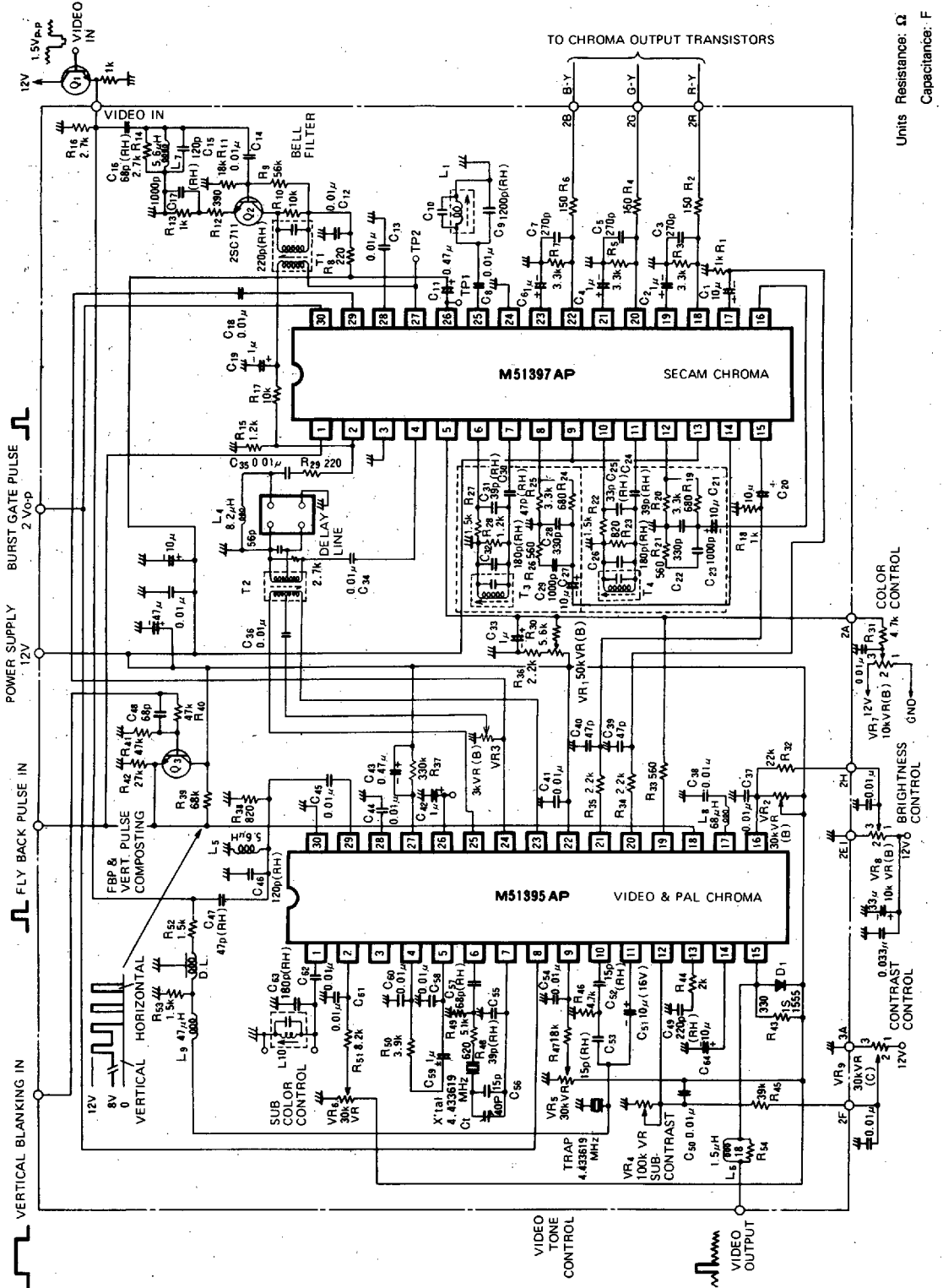
5. Burst cleaning coil "L<sub>10</sub>" (M51395AP)  
Apply PAL color signal to input.  
Adjust burst cleaning coil "L<sub>10</sub>" to give minimum chroma output signal value at pin 24.
6. Delay line transformer "T<sub>2</sub>", chroma difference signal control "VR<sub>3</sub>" (M51395AP)  
Adjust delay line transformer "T<sub>2</sub>" and chroma difference signal control "VR<sub>3</sub>" to correct demodulated ratios at pins 18, 20 and 22. If demodulated ratios are not correct, readjust burst cleaning coil "L<sub>10</sub>".



M51397AP

SECAM CHROMA SYSTEM

APPLICATION EXAMPLE



Units Resistance: Ω  
Capacitance: F

M51395AP M51397AP PWB  
PAL SECAM Dual System

Bottom View

