

DATA SHEET

TDA4852

Horizontal and vertical deflection
controller for autosync monitors

Preliminary specification
File under Integrated Circuits, IC02

December 1992

Horizontal and vertical deflection controller for autosync monitors

TDA4852

FEATURES

- Low jitter
- All adjustments DC-controllable
- Alignment-free oscillators
- Sync separators for video or horizontal and vertical TTL sync levels regardless of polarity
- Horizontal oscillator with PLL1 for sync and PLL2 for flyback
- Constant vertical and E/W amplitude in autosync operation
- DC-coupling to vertical power amplifier
- Internal supply voltage stabilization with excellent ripple rejection to ensure stable geometrical adjustments

GENERAL DESCRIPTION

The TDA4852 is a monolithic integrated circuit for economical solutions in autosync monitors. The IC incorporates the complete horizontal and vertical small signal processing. In conjunction with TDA4860/61/65, or TDA8351 (vertical output circuits) the ICs offer an extremely advanced system solution.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---------------|--|------|------|------|------|
| V_P | positive supply voltage (pin 1) | 9.2 | 12 | 16 | V |
| I_P | supply current | – | 40 | – | mA |
| $V_{i\ sync}$ | AC-coupled composite video signal with negative-going sync (peak-to-peak value, pin 9) | – | 1 | – | V |
| | sync slicing level | – | 120 | – | mV |
| | DC-coupled TTL-compatible horizontal sync signal (peak-to-peak value, pin 9) | 1.7 | – | – | V |
| | slicing level | 1.2 | 1.4 | 1.6 | V |
| | DC-coupled TTL-compatible vertical sync signal (peak-to-peak value, pin 10) | 1.7 | – | – | V |
| | slicing level | 1.2 | 1.4 | 1.6 | V |
| $I_{o\ V}$ | vertical differential output current (peak-to-peak value, pins 5 and 6) | – | 1 | – | mA |
| $I_{o\ H}$ | horizontal sink output current on pin 3 | – | – | 60 | mA |
| T_{amb} | operating ambient temperature range | 0 | – | +70 | °C |

ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|-------------------------|---------|-----------------|----------|-----------------------|
| | PINS | PIN POSITION | MATERIAL | CODE |
| TDA4852 | 20 | DIL | plastic | SOT146 ⁽¹⁾ |

Note

1. SOT146-1; 1996 November 27.

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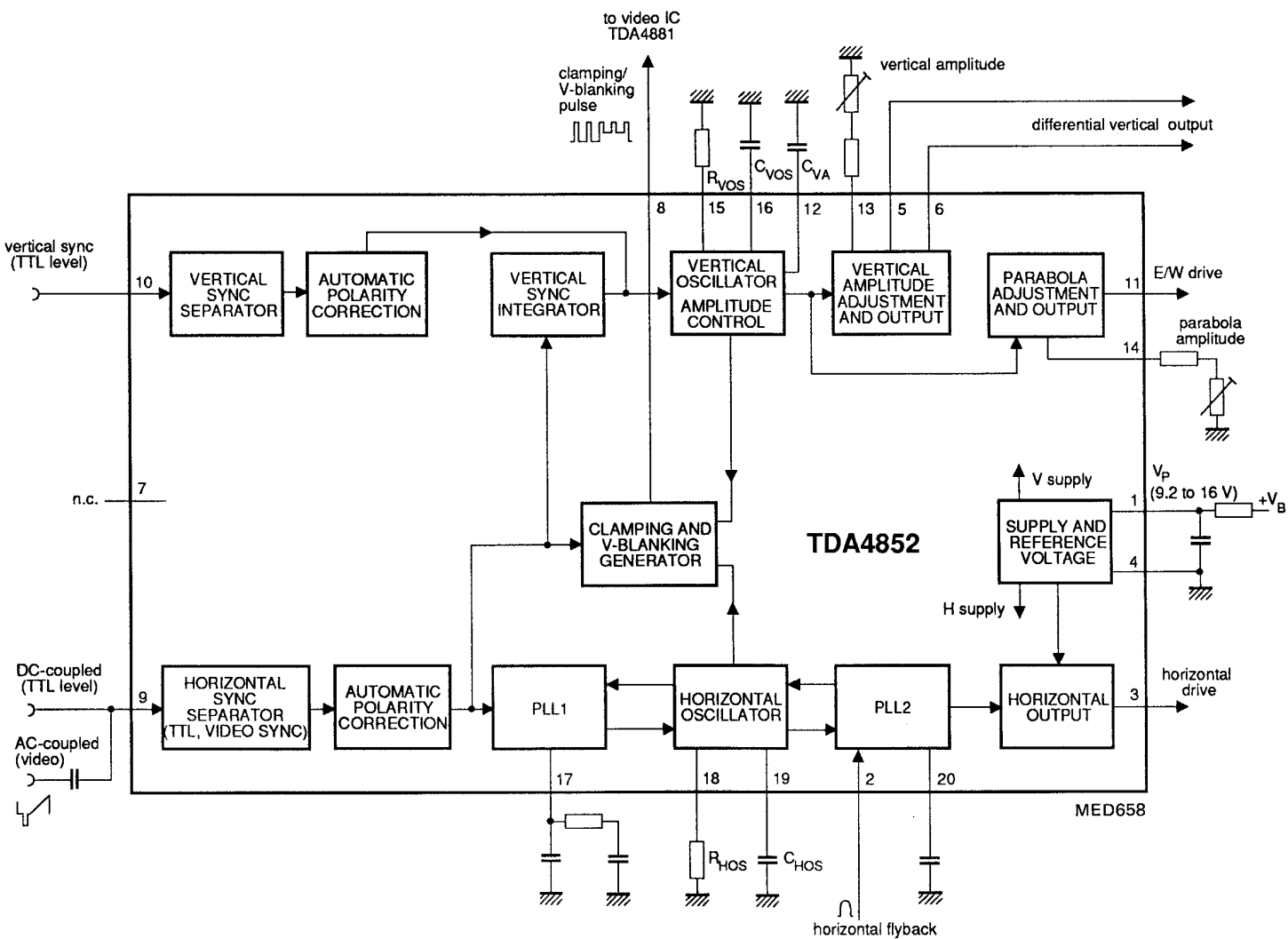


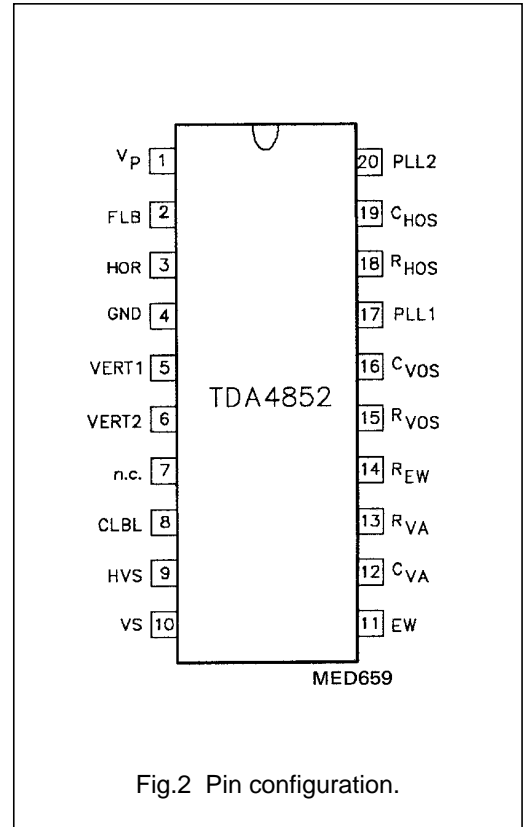
Fig.1 Block diagram.

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PINNING

| SYMBOL | PIN | DESCRIPTION |
|------------------|-----|--|
| V _P | 1 | positive supply voltage |
| FLB | 2 | horizontal flyback input |
| HOR | 3 | horizontal output |
| GND | 4 | ground (0 V) |
| VERT1 | 5 | vertical output 1; negative-going sawtooth |
| VERT2 | 6 | vertical output 2; positive-going sawtooth |
| n.c. | 7 | not connected |
| CLBL | 8 | clamping/blanking pulse output |
| HVS | 9 | horizontal sync/video input |
| VS | 10 | vertical sync input |
| EW | 11 | E/W output (parabola to driver stage) |
| C _{VA} | 12 | capacitor for amplitude control |
| R _{VA} | 13 | vertical amplitude adjustment input |
| R _{EW} | 14 | E/W amplitude adjustment input (parabola) |
| R _{VOS} | 15 | vertical oscillator resistor |
| C _{VOS} | 16 | vertical oscillator capacitor |
| PLL1 | 17 | PLL1 phase |
| R _{HOS} | 18 | horizontal oscillator resistor |
| C _{HOS} | 19 | horizontal oscillator capacitor |
| PLL2 | 20 | PLL2 phase |



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FUNCTIONAL DESCRIPTION

Horizontal sync separator and polarity correction

An AC-coupled video signal or a DC-coupled TTL sync signal (H only or composite sync) is input on pin 9. Video signals are clamped with top sync on 1.28 V, and are sliced at 1.4 V. This results in a fixed absolute slicing level of 120 mV related to top sync. DC-coupled TTL sync signals are also sliced at 1.4 V, however with the clamping circuit in current limitation. The polarity of the separated sync is detected by internal integration of the signal, then the polarity is corrected. The corrected sync is input signal for the vertical sync integrator and the PLL1 stage.

Vertical sync separator, polarity correction and vertical sync integrator

DC-coupled vertical TTL sync signals may be applied to pin 10. They are sliced at 1.4 V. The polarity of the separated sync is detected by internal integration, then the polarity is corrected. If pin 10 is not used, it must be connected to ground. The separated $V_{i\text{sync}}$ signal from pin 10, or the integrated composite sync signal from pin 9 (TTL or video) triggers directly the vertical oscillator.

Clamping and V-blanking generator

A combined clamping and V-blanking pulse is available on pin 8 (suitable for the video pre-amplifier TDA4881). The lower level of 1.9 V is the blanking signal derived from the vertical blanking pulse from the internal vertical oscillator. Vertical blanking starts with vertical sync and stops at the begin of vertical scan. By this, an optimum blanking is achieved. The upper level of 5.4 V is the horizontal clamping pulse with an internally fixed pulse width of 0.8 μs .

A monoflop, which is triggered by the trailing edge of the horizontal sync pulse, generates this pulse. If composite sync is applied, one clamping pulse per H-period is generated during V-sync. The phase of the clamping pulse may change during V-sync (see Fig.8).

PLL1 phase detector

The phase detector is a standard type using switched current sources. The middle of the sync is compared with a fixed point of the oscillator sawtooth voltage. The PLL filter is connected to pin 17. If composite sync is applied, the disturbed control voltage is corrected during V-sync (see Fig.8).

Horizontal oscillator

This oscillator is of the relaxation type and requires a fixed capacitor of 10 nF at pin 19. By changing the current into pin 18 the whole frequency range from 13 to 100 kHz can be covered. The current can be generated either by a frequency to voltage converter or by a resistor. A frequency adjustment may also be added if necessary. The PLL1 control voltage at pin 17 modulates via a buffer stage the oscillator thresholds. A high DC-loop gain ensures a stable phase relationship between horizontal sync and line flyback pulses.

PLL2 phase detector

This phase detector is similar to the PLL1 phase detector. Line flyback signals (pin 2) are compared with a fixed point of the oscillator sawtooth voltage. Delays in the horizontal deflection circuit are compensated by adjusting the phase relationship between horizontal sync and horizontal output pulses. A certain amount of phase adjustment is possible by injecting a DC current from an external source into the PLL2 filter capacitor at pin 20.

Horizontal driver

This open-collector output stage (pin 3) can directly drive an external driver transistor. The saturation voltage is less than 300 mV at 20 mA. To protect the line deflection transistor, the horizontal output stage does not conduct for $V_P < 6.4$ V (pin 1).

Vertical oscillator and amplitude control

This stage is designed for fast stabilization of the vertical amplitude after changes in sync conditions. The free-running frequency f_0 is determined by the values of R_{VOS} and C_{VOS} . The recommended values should be altered marginally only to preserve the excellent linearity and noise performance. The vertical drive currents I_5 and I_6 are in relation to the value of R_{VOS} . Therefore, the oscillator frequency must be determined only by C_{VOS} on pin 16.

$$f_0 = \frac{1}{10.8 \times R_{VOS} \times C_{VOS}}$$

To achieve a stabilized amplitude the free-running frequency f_0 (without adjustment) must be lower than the lowest occurring sync frequency. The following contributions can be assumed:

| | |
|---|-----------|
| minimum frequency offset between f_0 and the lowest trigger frequency | 10% |
| spread of IC | $\pm 3\%$ |
| spread of R (22 k Ω) | $\pm 1\%$ |
| spread of C (0.1 μF) | $\pm 5\%$ |
| | 19% |

$$\text{Result: } f_0 = \frac{50}{1.19} \text{ Hz} = 42 \text{ Hz}$$

(for 50 to 110 Hz application)

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-----------|--|------|-----------|--------------------|
| V_P | supply voltage (pin 1) | -0.5 | 16 | V |
| V_3 | voltage on pin 3 | -0.5 | 16 | V |
| V_8 | voltage on pin 8 | -0.5 | 7 | V |
| V_n | voltage on pins 5, 6, 9, 10, 13, 14 and 18 | -0.5 | 6.5 | V |
| I_2 | current on pin 2 | - | ± 10 | mA |
| I_3 | current on pin 3 | - | 100 | mA |
| I_8 | current on pin 8 | - | -10 | mA |
| T_{stg} | storage temperature range | -55 | +50 | $^{\circ}\text{C}$ |
| T_{amb} | operating ambient temperature range | 0 | 70 | $^{\circ}\text{C}$ |
| T_j | maximum junction temperature | 0 | +150 | $^{\circ}\text{C}$ |
| V_{ESD} | electrostatic handling for all pins (note 1) | - | ± 400 | V |

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

| SYMBOL | PARAMETER | THERMAL RESISTANCE |
|---------------|--------------------------------------|--------------------|
| $R_{th\ j-a}$ | from junction to ambient in free air | 65 K/W |

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CHARACTERISTICS

$V_P = 12\text{ V}$; $T_{\text{amb}} = +25\text{ }^\circ\text{C}$; measurements taken in Fig.3 unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|------|------|----------|--------------------|
| V_P | positive supply voltage (pin 1) | | 9.2 | 12 | 16 | V |
| I_P | supply current | $I_{18} = -1.05\text{ mA}$ | – | 36 | 44 | mA |
| | | $I_{18} = -3.388\text{ mA}$ | – | 40 | 49 | mA |
| Internal reference voltage | | | | | | |
| V_{ref} | internal reference voltage | | 6.0 | 6.25 | 6.5 | V |
| TC | temperature coefficient | $T_{\text{amb}} = +20\text{ to }+100\text{ }^\circ\text{C}$ | – | – | ± 90 | $10^{-6}/\text{K}$ |
| PSRR | power supply ripple rejection | $f = 1\text{ kHz sinewave}$ | 60 | 75 | – | dB |
| | | $f = 1\text{ MHz sinewave}$ | 25 | 35 | – | dB |
| V_P | supply voltage (pin 1) to ensure all internal reference voltages | | 9.2 | – | 16 | V |
| Composite sync input (AC-coupled) | | $V_{10} = 5\text{ V}$ | | | | |
| $V_{i\text{ sync}}$ | sync amplitude of video input signal (pin 9) | sync on green | – | 300 | – | mV |
| | top sync clamping level | | 1.1 | 1.28 | 1.5 | V |
| | slicing level above top sync level | $R_S = 50\ \Omega$ | 90 | 120 | 150 | mV |
| R_S | allowed source resistance for 7% duty factor | $V_{i\text{ sync}} > 200\text{ mV}$ | – | – | 1.5 | $\text{k}\Omega$ |
| r_g | differential input resistance | during sync | – | 80 | – | Ω |
| I_g | charging current of coupling capacitor | $V_g > 1.5\text{ V}$ | 1.3 | 2 | 3 | μA |
| t_{int} | vertical sync integration time to generate vertical trigger pulse | $f_H = 31\text{ kHz}$; $I_{18} = -1.050\text{ mA}$ | 7 | 10 | 13 | μs |
| | | $f_H = 64\text{ kHz}$; $I_{18} = -2.169\text{ mA}$ | 3.5 | 5 | 6.5 | μs |
| | | $f_H = 100\text{ kHz}$; $I_{18} = -3.388\text{ mA}$ | 2.5 | 3.4 | 4.5 | μs |
| Horizontal sync input (DC-coupled, TTL-compatible) | | | | | | |
| $V_{i\text{ sync}}$ | sync input signal (peak-to-peak value, pin 9) | | 1.7 | – | – | V |
| | slicing level | | 1.2 | 1.4 | 1.6 | V |
| t_p | minimum pulse width | | 700 | – | – | ns |
| t_r, t_f | rise time and fall time | | 10 | – | 500 | ns |
| I_g | input current | $V_g = 0.8\text{ V}$ | – | – | –200 | μA |
| | | $V_g = 5.5\text{ V}$ | – | – | 10 | μA |
| Automatic horizontal polarity switch | | H-sync on pin 9 | | | | |
| $t_{p\text{ H}/t_{\text{H}}}$ | horizontal sync pulse width related to t_{H} (duty factor for automatic polarity correction) | | – | – | 30 | % |
| t_p | delay time for changing sync polarity | | 0.3 | – | 1.8 | ms |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|--|--------------------|--------------------|-----------|---------------|
| Vertical sync input (DC-coupled, TTL-compatible) | | V-sync on pin 10 | | | | |
| $V_{i\text{ sync}}$ | sync input signal (peak-to-peak value, pin 10) | | 1.7 | – | – | V |
| | slicing level | | 1.2 | 1.4 | 1.6 | V |
| I_{10} | input current | $0 < V_{10} < 5.5\text{ V}$ | – | – | ± 10 | μA |
| $t_{p\text{ v}}$ | maximum vertical sync pulse width for automatic vertical polarity switch | | – | – | 300 | μs |
| Horizontal clamping / blanking generator output | | Fig.6 | | | | |
| V_8 | output voltage LOW | | – | – | 0.9 | V |
| | blanking output voltage | internal V blanking | 1.6 | 1.9 | 2.2 | V |
| | clamping output voltage | H-sync on pin 9 | 5.15 | 5.4 | 5.65 | V |
| I_8 | internal sink current for all output levels | H and V scanning | 2.3 | 2.9 | 3.5 | mA |
| | external load current | | – | – | –3.0 | mA |
| t_8 | clamping pulse start | | with end of H-sync | | | |
| t_{clp} | clamping pulse width | $V_8 = 3\text{ V}$ | 0.6 | 0.8 | 1.0 | μs |
| S | steepness of rise and fall times | | – | 60 | 75 | ns/V |
| Vertical oscillator | | $V_{\text{ref}} = 6.25\text{ V}$ | | | | |
| f_0 | vertical free-running frequency | $R_{15} = 22\text{ k}\Omega$; $C_{16} = 0.1\text{ }\mu\text{F}$ | – | 42 | – | Hz |
| f_v | nominal vertical sync range | no f_0 adjustment | 50 | – | 110 | Hz |
| V_{15} | voltage on pin 15 | $R_{15} = 22\text{ k}\Omega$ | 2.8 | 3.0 | 3.2 | V |
| t_d | delay between sync pulse and start of vertical scan | measured on pin 8 | 240 | 300 | 360 | μs |
| I_{12} | control current for amplitude control | | – | ± 200 | – | μA |
| C_{12} | capacitor for amplitude control | | – | – | 0.18 | μF |
| Vertical differential output | | Fig.7 | | | | |
| I_o | differential output current between pins 5 and 6 (peak-to-peak value) | mode 3; $I_{13} > -135\text{ }\mu\text{A}$; $R_{15} = 22\text{ k}\Omega$ | 0.9 | 1.0 | 1.1 | mA |
| | maximum offset-current error | $I_o = 1\text{ mA}$ | – | – | ± 2.5 | % |
| | maximum linearity error | | – | – | ± 1.5 | % |
| Vertical amplitude adjustment (in percentage of output signal) | | | | | | |
| V_{13} | input voltage | | – | 5.0 | – | V |
| I_{13} | adjustment current | $I_{o\text{ max}}$ (100%) | –110 | –120 | –135 | μA |
| | | $I_{o\text{ min}}$ (typically 58%) | – | 0 | – | μA |
| Horizontal comparator PLL1 | | | | | | |
| V_{17} | upper control voltage limitation | | – | 5.9 | – | V |
| | lower control voltage limitation | | – | 5.1 | – | V |
| I_{17} | control current | Fig.6 | – | $\pm 0.083 I_{18}$ | – | mA |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|--|--|------|----------------------------------|------|---------------------|
| Horizontal oscillator | | | | | | |
| f _{osc} | centre frequency | R ₁₈ = 2.4 kΩ (pin 18); C ₁₉ = 10 nF (pin 19) | – | 31.45 | – | kHz |
| | deviation of centre frequency | | – | – | ±3 | % |
| | temperature coefficient | | 0 | +200 | +300 | 10 ⁻⁶ /K |
| φ _H /t _H | relative holding/catching range | | ±6 | ±6.5 | ±7.3 | % |
| I ₁₈ | external oscillator current | | -0.5 | – | -4.3 | mA |
| V ₁₈ | voltage at reference current input (pin18) | | 2.35 | 2.5 | 2.65 | V |
| Horizontal PLL2 | | Fig.6 | | | | |
| V ₂ | upper clamping level of flyback input | I ₂ = 6 mA | – | 5.5 | – | V |
| | lower clamping level of flyback input | I ₂ = -1 mA | – | -0.75 | – | V |
| | H-flyback slicing level | | – | 3.0 | – | V |
| t _d /t _H | delay between middle of sync and middle of H-flyback related to t _H | | – | 3.0 | – | % |
| V ₂₀ | upper control voltage limitation | | – | 6.2 | – | V |
| | lower control voltage limitation | | – | 4.8 | – | V |
| I ₂₀ | control current | | – | ±0.083 _{I₁₈} | – | μA |
| Δt/t _H | PLL2 control range related to t _H | | 30 | – | – | % |
| Horizontal output (open-collector) | | Fig.6 | | | | |
| V ₃ | output voltage LOW | I ₃ = 20 mA | – | – | 0.3 | V |
| | | I ₃ = 60 mA | – | – | 0.8 | V |
| t _p /t _H | t _H duty factor | | 42 | 45 | 48 | % |
| V _P | threshold to activate under voltage protection | horizontal output off | – | 5.6 | – | V |
| | | horizontal output on | – | 5.8 | – | V |
| Δt _H | jitter of horizontal output | f = 31 kHz | – | – | 3.5 | ns |
| | | f = 64 kHz | – | – | 1.9 | ns |
| | | f = 100 kHz | – | – | 1.2 | ns |
| E/W output | | note 1 | | | | |
| V ₁₁ | bottom output signal during mid-scan (pin 11) | internally stabilized | 1.05 | 1.2 | 1.35 | V |
| | top output signal during flyback | | 4.2 | 4.5 | 4.8 | V |
| | temperature coefficient of output signal | | – | – | 250 | 10 ⁻⁶ /K |
| E/W amplitude adjustment (parabola) | | Fig.7 | | | | |
| V ₁₄ | input voltage (pin 14) | | – | 5.0 | – | V |
| I ₁₄ | adjustment current | 100% parabola | -110 | -120 | -135 | μA |
| | | typically 28% parabola | – | 0 | – | μA |

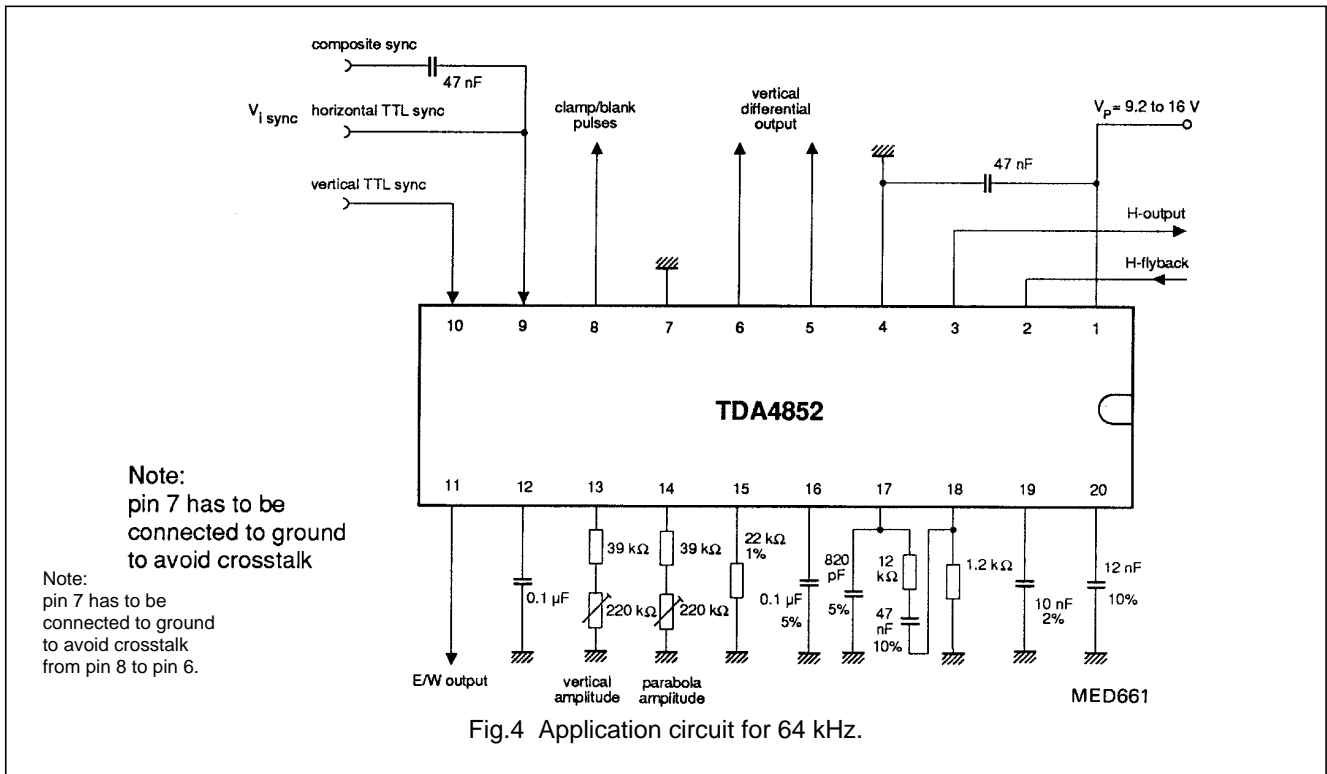
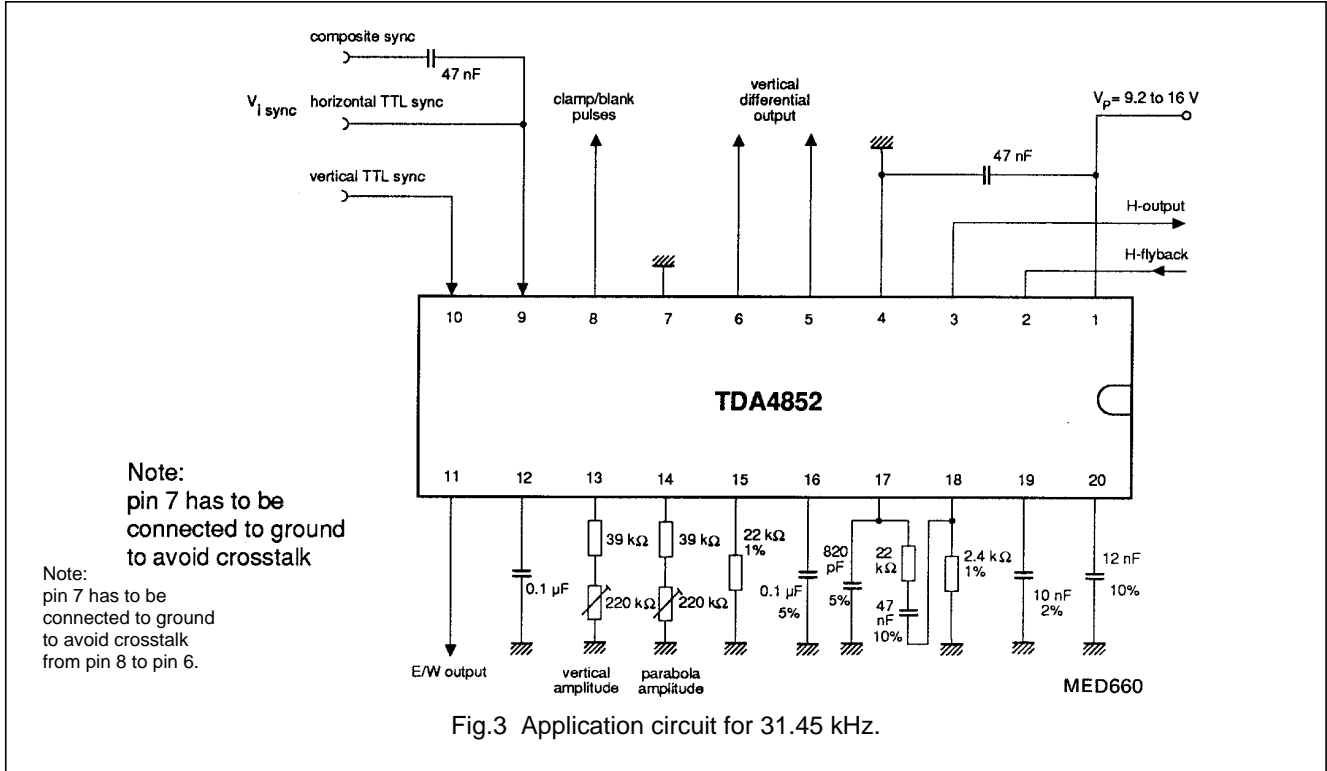
Note to the characteristics

1. Parabola amplitude does not track with vertical amplitude adjustment. Tracking can be achieved by a resistor from vertical amplitude potentiometer to pin 14.

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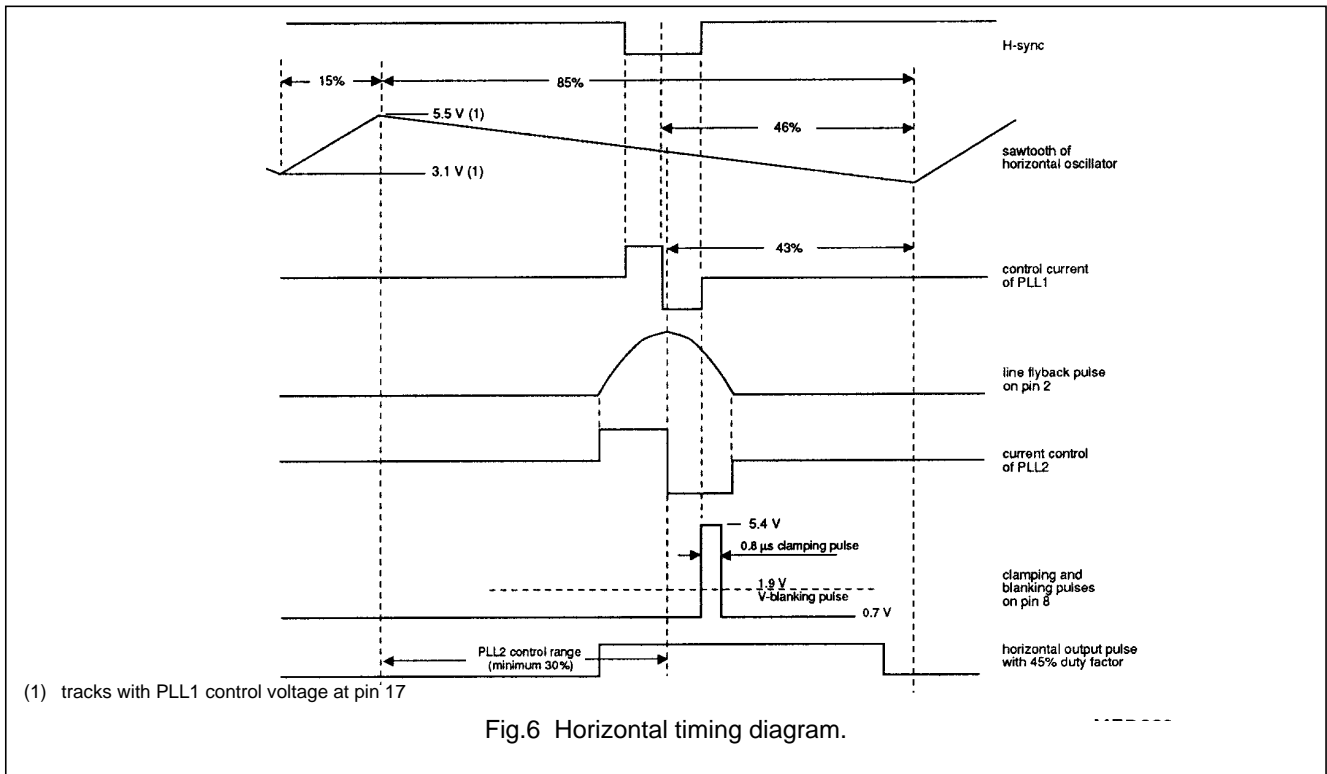
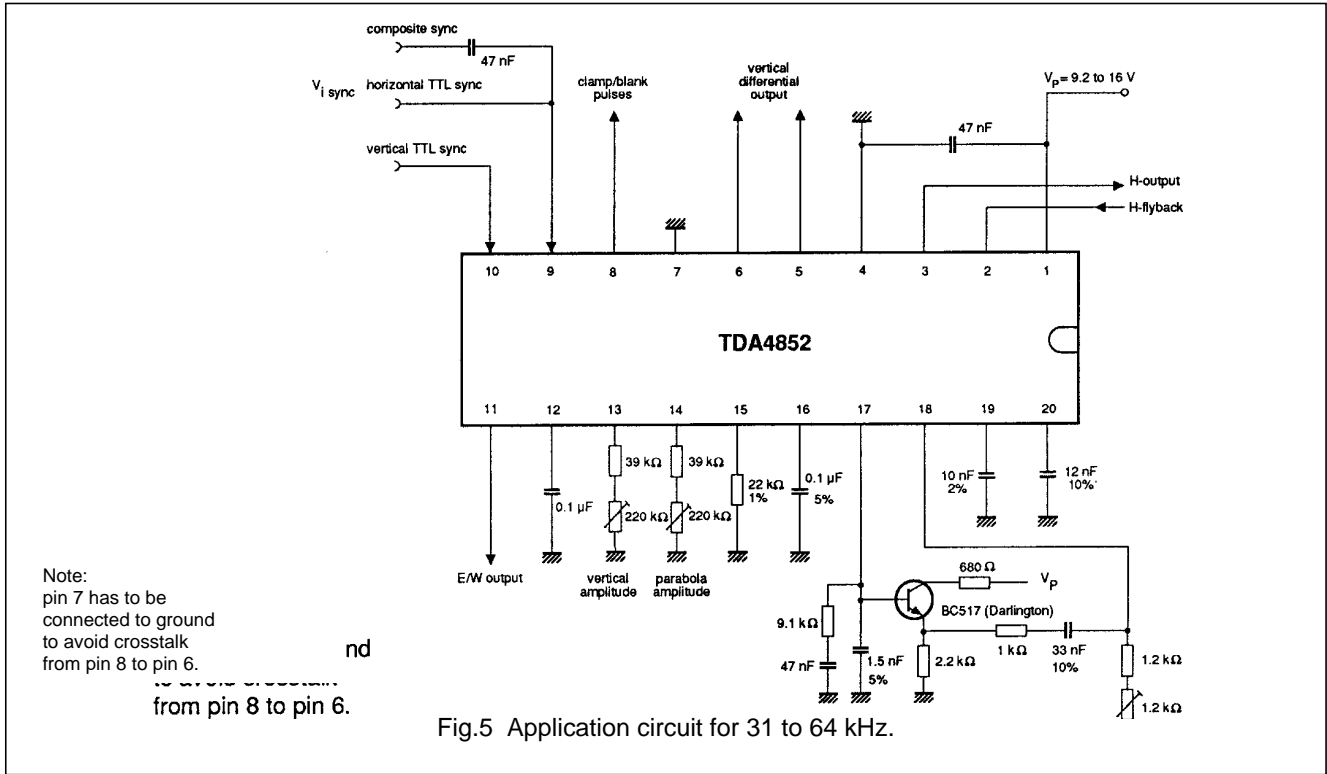
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APPLICATION INFORMATION



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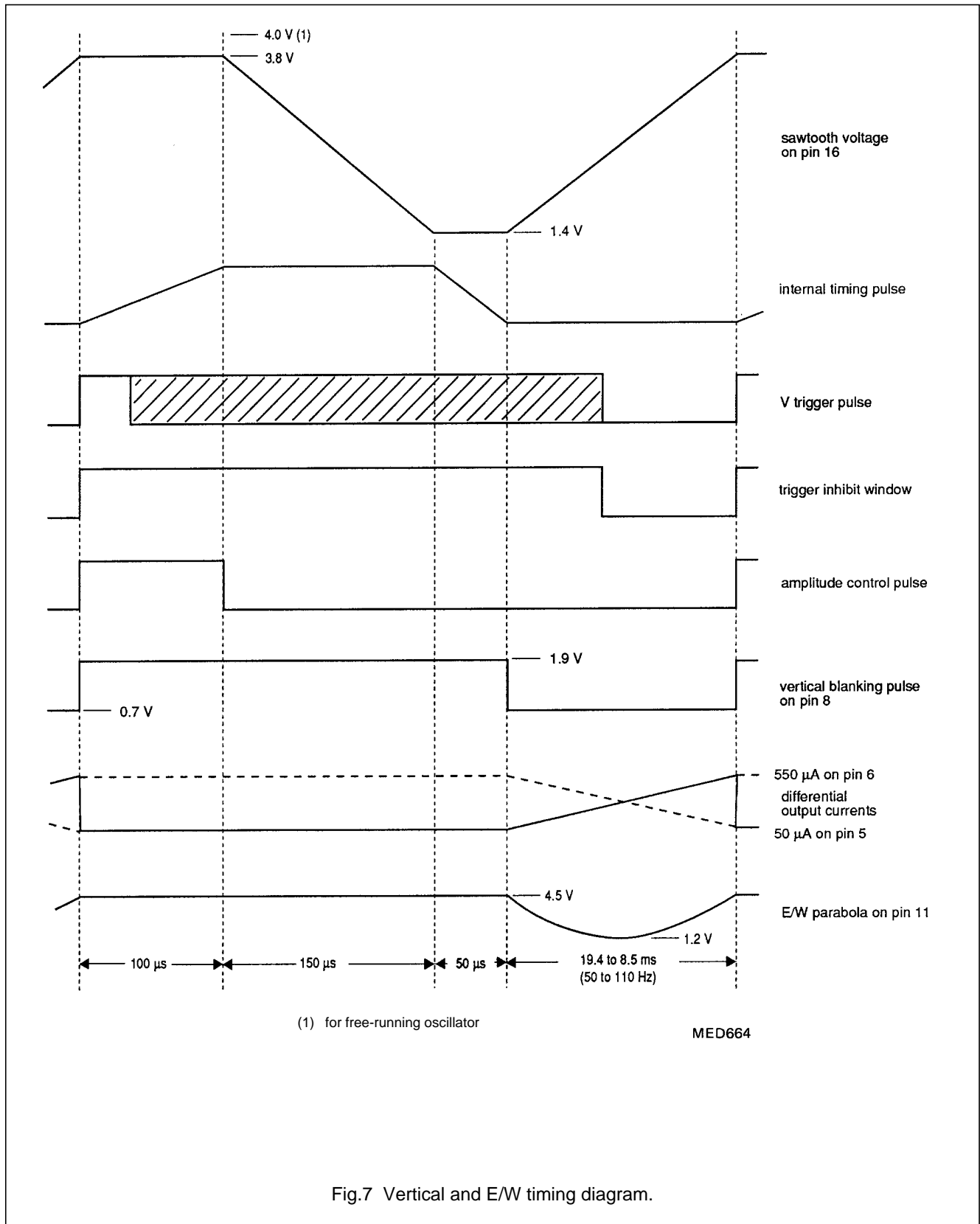
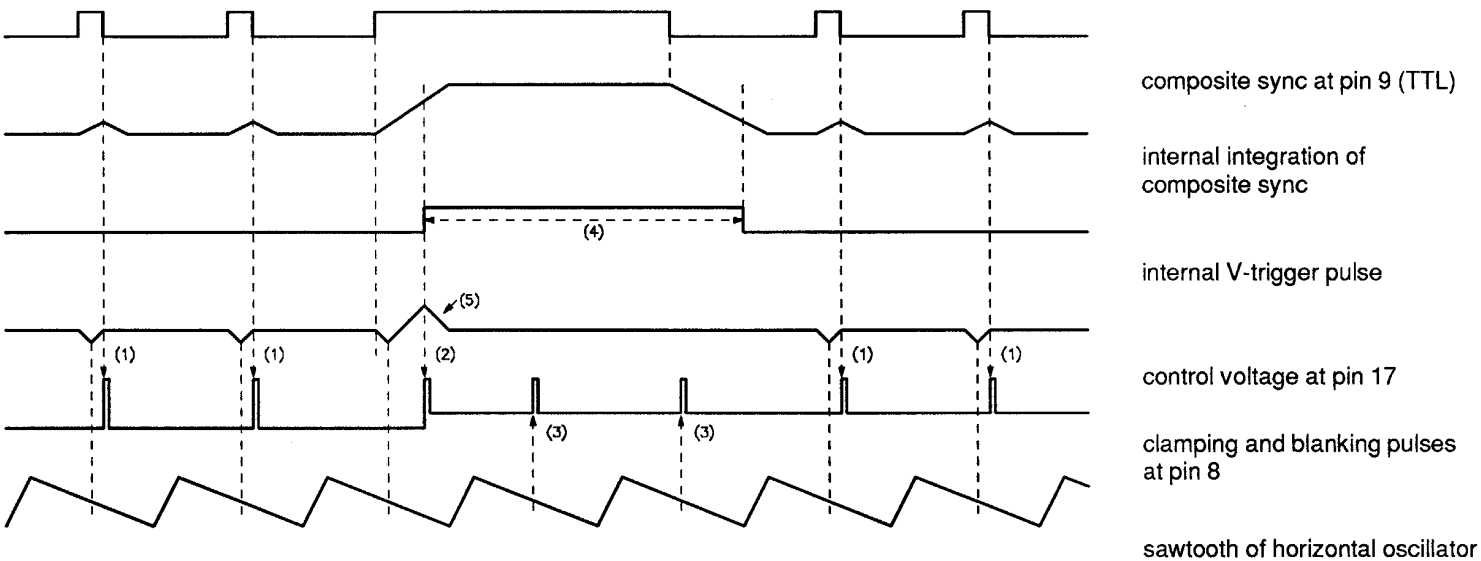


Fig.7 Vertical and E/W timing diagram.

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MED665

- (1) clamp pulses triggered by H-sync
- (2) clamp pulses triggered by leading edge of V-trigger pulse
- (3) clamp pulses triggered by horizontal oscillator
- (4) during V-trigger pulse clamp pulses are generated internally
- (5) control voltage of PLL1 is corrected during V-trigger pulse

Fig.8 Pulse diagram for composite sync applications (showing reduced influence of V-sync on H-phase and drive pulses for F/V converters).

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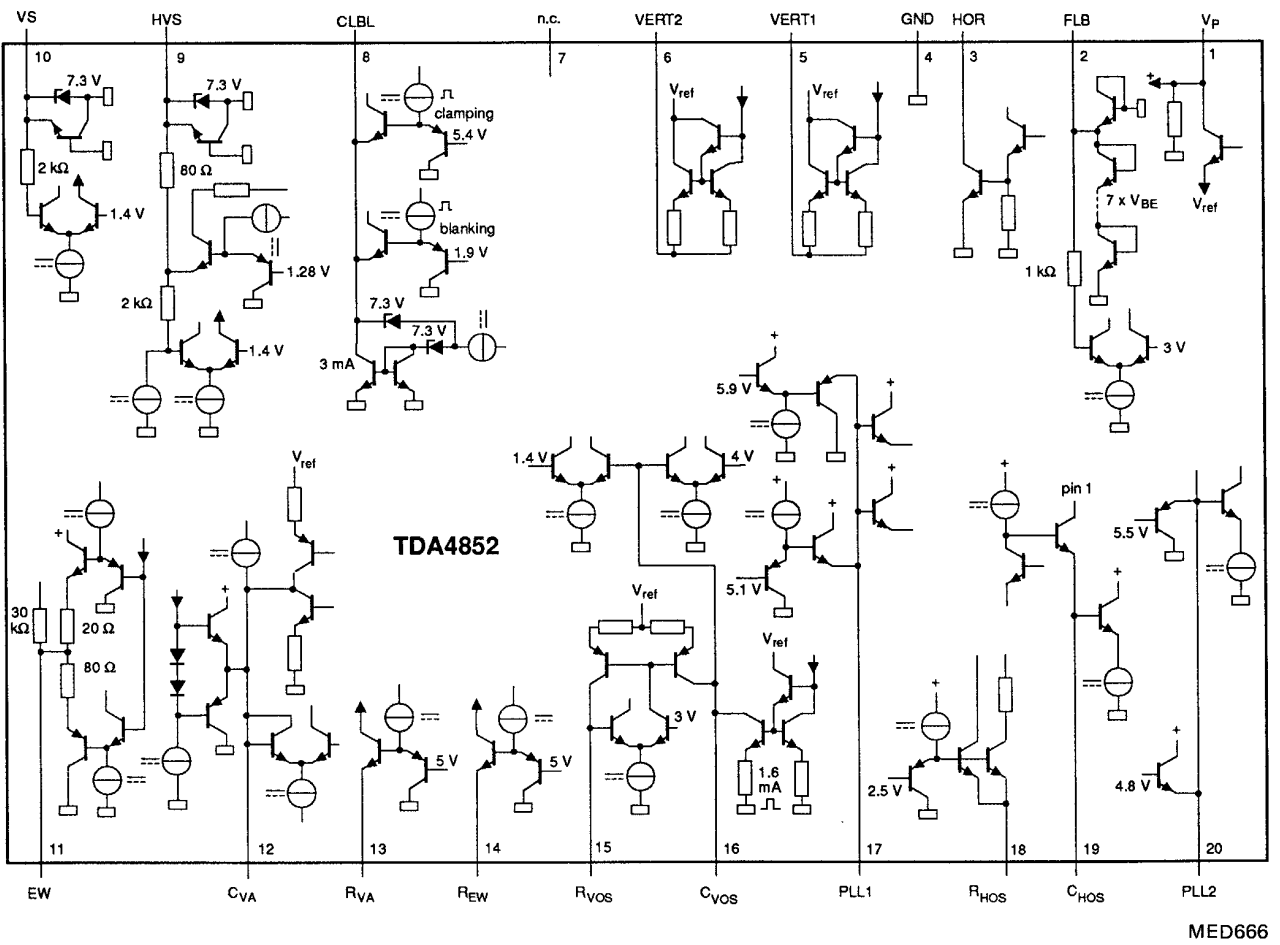
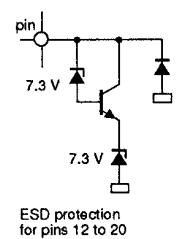
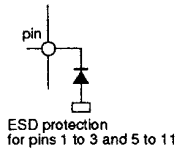


Fig.9 Internal circuits.



MED666

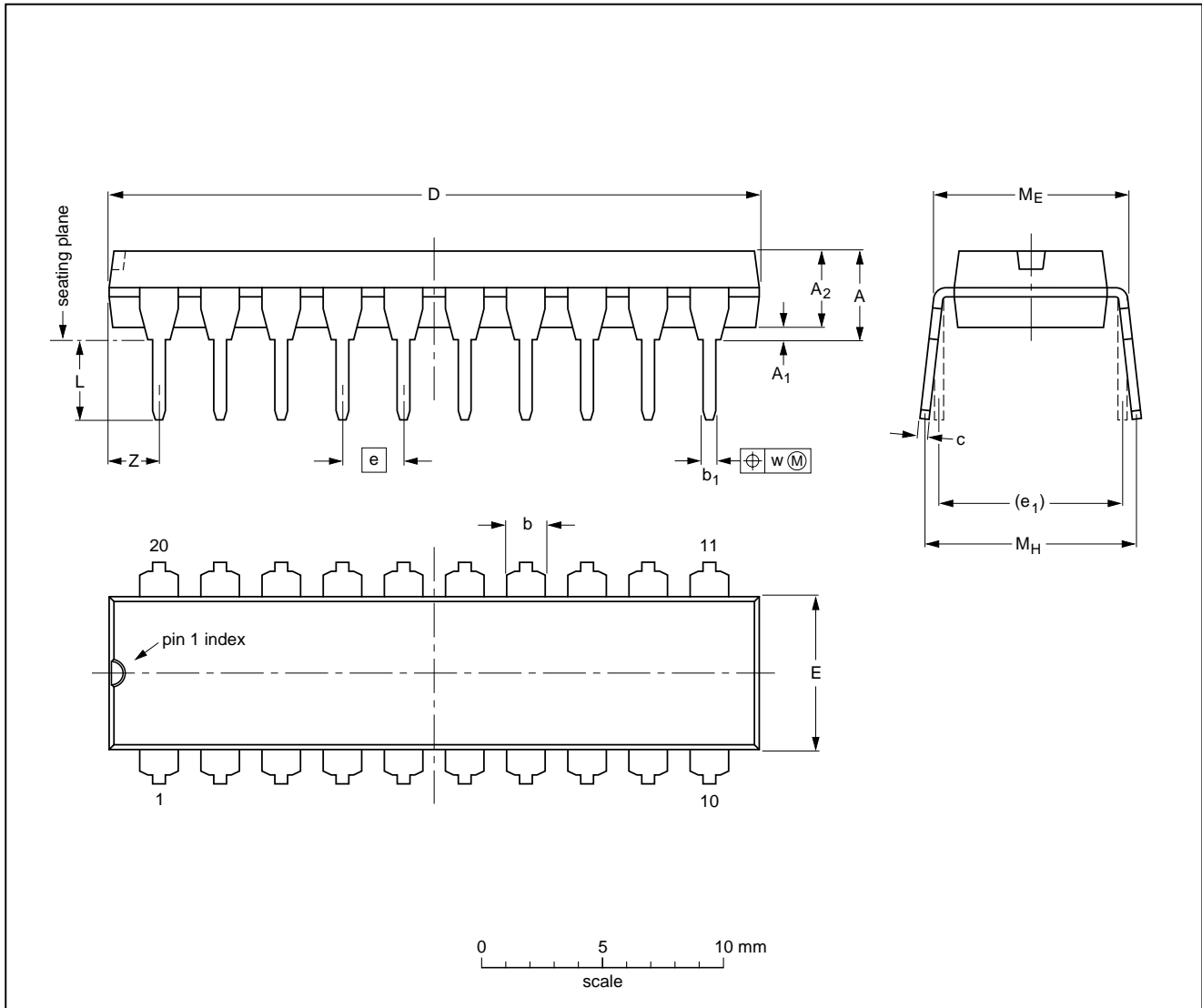
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PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.30 | 0.53 0.38 | 0.36 0.23 | 26.92 26.54 | 6.40 6.22 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 2.0 |
| inches | 0.17 | 0.020 | 0.13 | 0.068 0.051 | 0.021 0.015 | 0.014 0.009 | 1.060 1.045 | 0.25 0.24 | 0.10 | 0.30 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.078 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT146-1 | | | SC603 | | | 92-11-17 95-05-24 |

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact

with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

| | |
|---|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

LIFE SUPPORT APPLICATIONS

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