



SBOS247B - JUNE 2002 - REVISED FEBRUARY 2005

Low-Noise, Low-Distortion INSTRUMENTATION AMPLIFIER Replacement for SSM2017

FEATURES

- LOW NOISE: 1.3nV/\Hz at 1kHz
- LOW THD+N: 0.004% at 1kHz, G = 100
- WIDE BANDWIDTH: 800kHz at G = 100
- WIDE SUPPLY RANGE: ±4.5V to ±18V
- HIGH CMR: > 100dB
- GAIN SET WITH EXTERNAL RESISTOR
- DIP-8 AND SOL-16 WIDEBODY PACKAGES

APPLICATIONS

- PROFESSIONAL MICROPHONE PREAMPS
- MOVING-COIL TRANSDUCER AMPLIFIERS
- DIFFERENTIAL RECEIVERS
- BRIDGE TRANSDUCER AMPLIFIERS

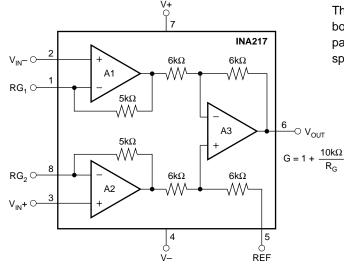
DESCRIPTION

The INA217 is a low-noise, low-distortion, monolithic instrumentation amplifier. Current-feedback circuitry allows the INA217 to achieve wide bandwidth and excellent dynamic response over a wide range of gain. The INA217 is ideal for low-level audio signals such as balanced low-impedance microphones. Many industrial, instrumentation, and medical applications also benefit from its low noise and wide bandwidth.

Unique distortion cancellation circuitry reduces distortion to extremely low levels, even in high gain. The INA217 provides near-theoretical noise performance for 200 Ω source impedance. The INA217 features differential input, low noise, and low distortion that provides superior performance in professional microphone amplifier applications.

The INA217 features wide supply voltage, excellent output voltage swing, and high output current drive, making it an optimal candidate for use in high-level audio stages.

The INA217 is available in the same DIP-8 and SOL-16 wide body packages and pinouts as the SSM2017. For a smaller package, see the INA163 in SO-14 narrow. The INA217 is specified over the temperature range of -40° C to $+85^{\circ}$ C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ABSOLUTE MAXIMUM RATINGS(1)

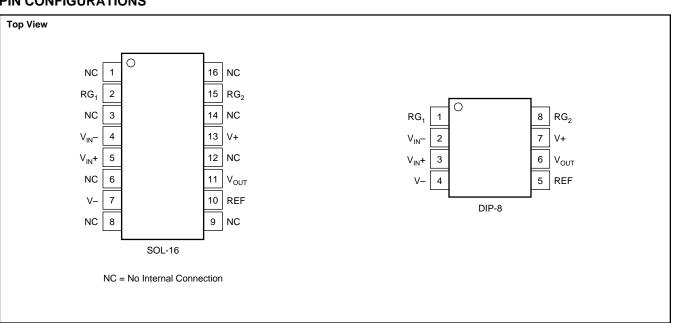
NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA217	SOL-16	DW	INA217
INA217	DIP-8	Р	INA217

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATIONS



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS: V_S = $\pm 15V$

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

 T_{A} = +25°C, R_{L} = 2k\Omega, V_{S} = $\pm 15V,$ unless otherwise noted.

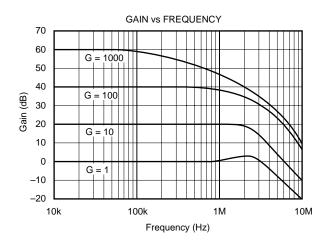
PARAMETER	CONDITIONS	MIN	ТҮР	МАХ	UNITS
GAIN EQUATION			$G = 1 + 10k/R_{G}$		
Range			1 to 10000		V/V
Gain Error, G = 1			±0.1	±0.25	%
G = 10			±0.2	±0.7	%
G = 100			±0.2		%
G = 1000			±0.5		%
Gain Temp Drift Coefficient, G = 1			±3	±10	ppm/°C
G > 10			±40	±100	ppm/°C
Nonlinearity, $G = 1$			±0.0003		% of FS
G = 100			±0.0006		% of FS
INPUT STAGE NOISE					
Voltage Noise	$R_{SOURCE} = 0\Omega$				
f _O = 1kHz			1.3		nV/√Hz
$f_0 = 100Hz$			1.5		nV/√Hz
$f_0 = 10Hz$			3.5		nV/√Hz
Current Noise					
$f_{O} = 1 \text{kHz}$			0.8		pA/√Hz
OUTPUT STAGE NOISE					
Voltage Noise, f _O = 1kHz			90		nV/√Hz
			50 . 0000/0	250 . 5000/0	
Input Offset Voltage	$V_{CM} = V_{OUT} = 0V$		50 + 2000/G	250 + 5000/G	μV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		1 + 20/G	0.000/0	μ ν/°C
vs Power Supply	$V_{S} = \pm 4.5V$ to $\pm 18V$		1 + 50/G	3 + 200/G	μV/V
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range	$V_{IN} + - V_{IN} - = 0V$	(V+) – 4	(V+) – 3		V
	$V_{IN} + - V_{IN} - = 0V$	(V–) + 4	(V–) + 3		V
Common-Mode Rejection, G = 1	$V_{CM} = \pm 11V, R_{SBC} = 0\Omega$	70	80		dB
G = 100		100	116		dB
INPUT BIAS CURRENT					
Initial Bias Current			2	12	μA
vs Temperature			10		nA/°C
Initial Offset Current			0.1	1	μA
vs Temperature			0.5		nA/°C
INPUT IMPEDANCE					
	Differential		60 2		MΩ pF
	Common-Mode		60 2		MΩ pF
Bandwidth, Small Signal, -3dB, G = 1			3.4		MHz
G = 100			800		kHz
Slew Rate			15		V/µs
THD+Noise, f = 1kHz	G = 100		0.004		%
Settling Time, 0.1%	G = 100, 10V Step		2		μs
0.01%	G = 100, 10V Step		3.5		μs
Overload Recovery	50% Overdrive		1		μs
OUTPUT					
Voltage	R _L to GND	(V+) – 2	(V+) – 1.8		V
		(V–) + 2	(V–) + 1.8		V
Load Capacitance Stability			1000		pF
Short-Circuit Current	Continuous-to-Common		±60		mA
POWER SUPPLY					
Rated Voltage			±15		V
Voltage Range		±4.5		±18	V
Current, Quiescent	$I_{O} = 0mA$		±10	±12	mA
TEMPERATURE RANGE					
Specification		-40		+85	°C
Operating		-40		+125	°C
Thermal Resistance					
DIP-8 $ heta_{JA}$			+85		°C/W
SOL-16		1	+90		°C/W

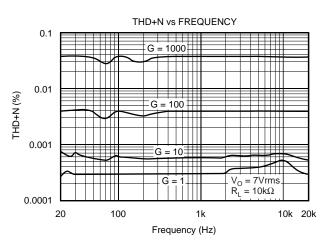
NOTE: (1) Gain accuracy is a function of external R_G .

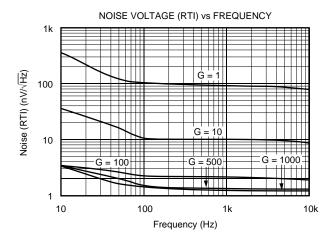


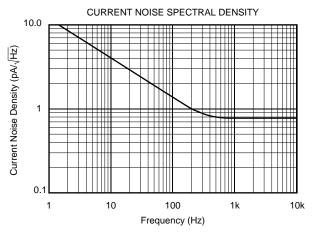
TYPICAL CHARACTERISTICS

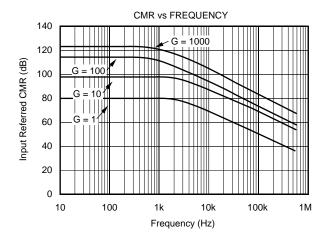
At T_A = +25°C, V_S = $\pm 15V$, R_L = 2k Ω , unless otherwise noted.

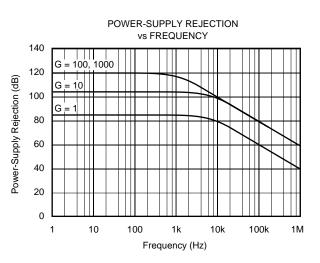








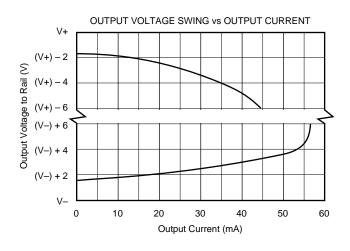


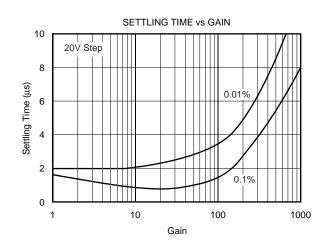




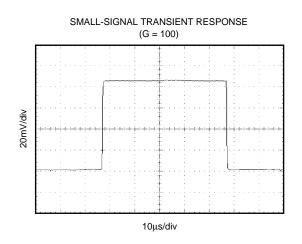
TYPICAL CHARACTERISTICS (Cont.)

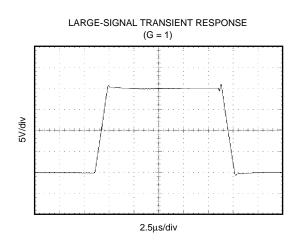
At T_A = +25°C, V_S = $\pm 15V$, R_L = 2k Ω , unless otherwise noted.

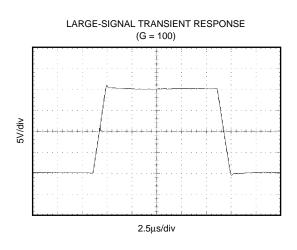




SMALL-SIGNAL TRANSIENT RESPONSE (G = 1)











APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation. Power supplies should be bypassed with 0.1μ F tantalum capacitors near the device pins. The output Reference (pin 5) should be a low-impedance connection. Resistance of a few ohms in series with this connection will degrade the common-mode rejection of the INA217.

GAIN-SET RESISTOR

Gain is set with an external resistor, R_G, as shown in Figure 1. The two internal $5k\Omega$ feedback resistors are laser-trimmed to $5k\Omega$ within approximately ±0.2%. The gain equation for the INA217 is:

$$G = 1 + \frac{10,000}{R_G}$$

The temperature coefficient of the internal 5k Ω resistors is approximately ±25ppm/°C. Accuracy and TCR of the external R_G will also contribute to gain error and temperature drift. These effects can be inferred from the gain equation. Make a short, direct connection to the gain set resistor, R_G. Avoid running output signals near these sensitive input nodes.

NOISE PERFORMANCE

The INA217 provides very low noise with low-source impedance. Its $1.3nV/\sqrt{Hz}$ voltage noise delivers near-theoretical noise performance with a source impedance of 200Ω . The input stage design used to achieve this low noise results in

relatively high input bias current and input bias current noise. As a result, the INA217 may not provide the best noise performance with a source impedance greater than $10k\Omega$. For source impedance greater than $10k\Omega$, other instrumentation amplifiers may provide improved noise performance.

INPUT CONSIDERATIONS

Very low source impedance (less than 10Ω) can cause the INA217 to oscillate. This depends on circuit layout, signal source, and input cable characteristics. An input network consisting of a small inductor and resistor, as shown in Figure 2, can greatly reduce any tendency to oscillate. This is especially useful if a variety of input sources are to be connected to the INA217. Although not shown in other figures, this network can be used as needed with all applications shown.

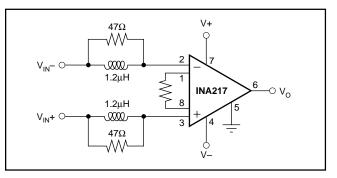


FIGURE 2. Input Stabilization Network.

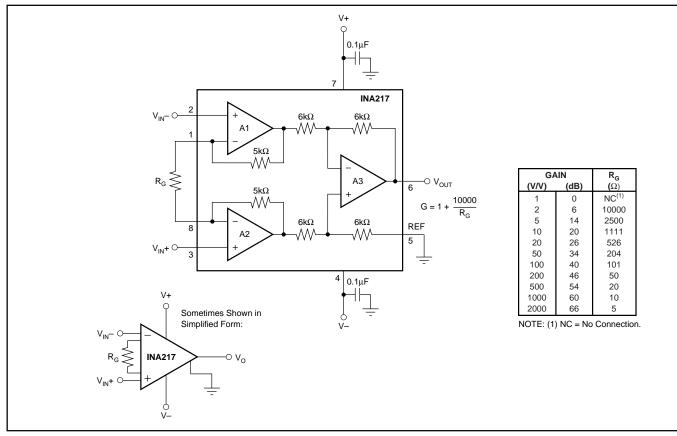


FIGURE 1. Basic Circuit Connections.



OFFSET VOLTAGE TRIM

A variable voltage applied to pin 5, as shown in Figure 3, can be used to adjust the output offset voltage. A voltage applied to pin 5 is summed with the output signal. An op amp connected as a buffer is used to provide a low impedance at pin 5 to assure good common-mode rejection.

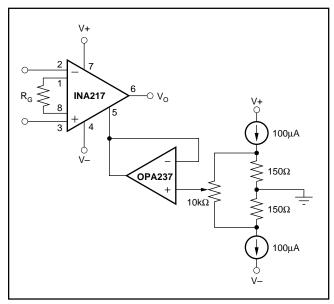


FIGURE 3. Offset Voltage Adjustment Circuit.

MICROPHONE AMPLIFIER

Figure 4 shows a typical circuit for a professional microphone input amplifier. R_1 and R_2 provide a current path for conventional 48V phantom power source for a remotely located microphone. An optional switch allows phantom power to be disabled. C_1 and C_2 block the phantom power voltage from the INA217 input circuitry. Non-polarized capacitors should be used for C_1 and C_2 if phantom power is to be disabled. For additional input protection against ESD and hot-plugging, four IN4148 diodes may be connected from the input to supply lines.

 R_4 and R_5 provide a path for input bias current of the INA217. Input offset current (typically 100nA) creates a DC differential input voltage that will produce an output offset voltage. This is generally the dominant source of output offset voltage in this application. With a maximum gain of 1000 (60dB), the output offset voltage can be several volts. This may be entirely acceptable if the output is AC-coupled into the subsequent stage. An alternate technique is shown in Figure 4. An inexpensive FET-input op amp in a feedback loop drives the DC output voltage to 0V. A2 is not in the audio signal path and does not affect signal quality.

Gain is set with a variable resistor, R₇, in series with R₆. R₆ determines the maximum gain. The total resistance, R₆ + R₇, determines the lowest gain. A special reverse-log taper potentiometer for R₇ can be used to create a linear change (in dB) with rotation.

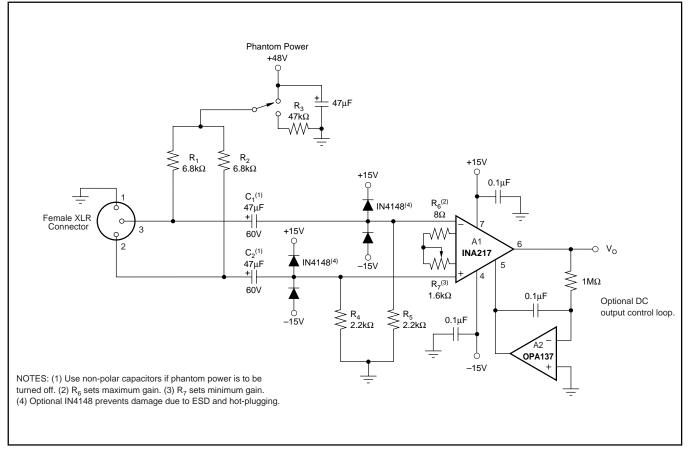


FIGURE 4. Phantom-Powered Microphone Preamplifier.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
INA217AIDWR	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA217AIDWRE4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA217AIDWT	ACTIVE	SOIC	DW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA217AIDWTE4	ACTIVE	SOIC	DW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA217AIP	ACTIVE	PDIP	Р	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA217AIPG4	ACTIVE	PDIP	Р	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*A	Il dimensions are nominal												
	Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	INA217AIDWR	SOIC	DW	16	1000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
	INA217AIDWT	SOIC	DW	16	250	180.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA217AIDWR	SOIC	DW	16	1000	346.0	346.0	33.0
INA217AIDWT	SOIC	DW	16	250	184.0	184.0	50.0

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AA.



MECHANICAL DATA

MPDI001A - JANUARY 1995 - REVISED JUNE 1999



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



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